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# P-Channel 20 V (D-S) MOSFET

#### **DESCRIPTION**

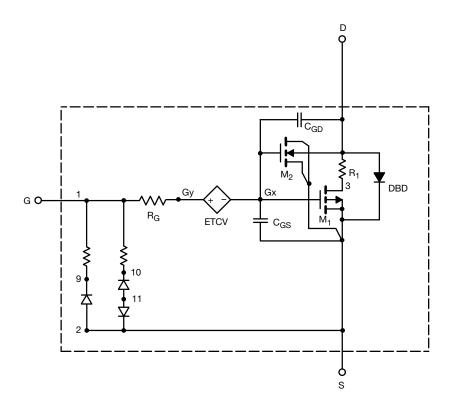
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55  $^{\circ}\text{C}$  to +125  $^{\circ}\text{C}$  temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{\rm gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### **CHARACTERISTICS**

- P-Channel Vertical DMOS
- Macro Model (Sub-circuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 °C to +125 °C Temperature Range
- · Model the Gate Charge

#### SUBCIRCUIT MODEL SCHEMATIC



#### Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



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<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = -250 \mu A$	0.63	-	٧
Drain-Source On-State Resistance a	R <sub>DS(on)</sub>	$V_{GS} = -4.5 \text{ V}, I_D = -4 \text{ A}$	0.0230	0.0265	Ω
		$V_{GS} = -2.5 \text{ V}, I_D = -4 \text{ A}$	0.0360	0.0340	
Diode Forward Voltage	$V_{SD}$	I <sub>S</sub> = -3.6 A	-0.8	-0.8	V
Dynamic <sup>b</sup>					
Total Gate Charge	Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	$V_{DS} = -10 \text{ V}, V_{GS} = -8 \text{ V}, I_D = -4.5 \text{ A}$	18	23.8	
			11	13.8	nC
Gate-Source Charge		$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -4.5 \text{ A}$	1.9	1.9	, IIC
Gate-Drain Charge			3	3	

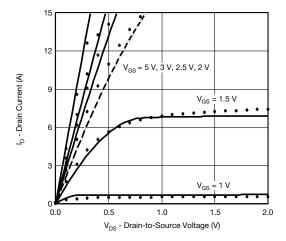
#### Notes

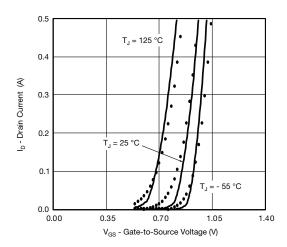
- a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

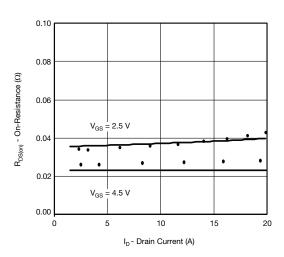
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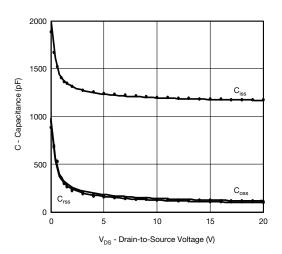
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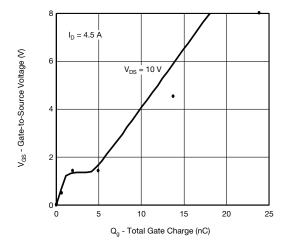
## **COMPARISON OF MODEL WITH MEASURED DATA** ( $T_J = 25~^{\circ}\text{C}$ , unless otherwise noted)

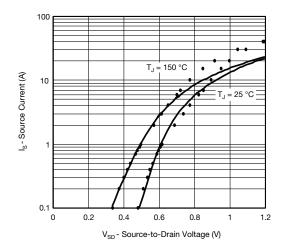












#### Note

Dots and squares represent measured data.
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