SPICE Device Model SQJ844AEP

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Vishay Siliconix

Dual N-Channel 30 V (D-S) 175 °C MOSFET

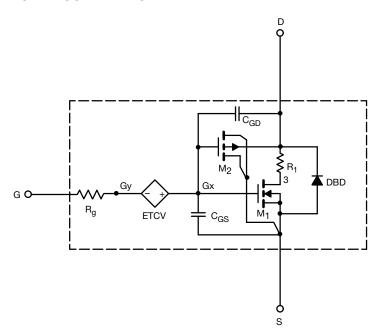
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Sub-circuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 °C to +125 °C Temperature Range
- Model the Gate Charge



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

SUBCIRCUIT MODEL SCHEMATIC



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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	2	2	V
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 7.6 \text{ A}$	0.0150	0.0138	Ω
		$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 5.9 \text{ A}$	0.0250	0.0230	
Forward Transconductance ^a	g _{fs}	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 7.6 \text{ A}$	18	20	S
Diode Forward Voltage	V _{SD}	I _S = 4.3 A	0.8	0.8	V
Dynamic ^b					
Input Capacitance	Ciss	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	954	929	pF
Output Capacitance	C _{oss}		280	280	
Reverse Transfer Capacitance	C _{rss}		93	93	
Total Gate Charge	Qg	V_{DS} = 15 V, V_{GS} = 10 V, I_{D} = 10 A	15	17	nC
Gate-Source Charge	Q _{gs}		3	3	
Gate-Drain Charge	Q _{gd}		3	3	

Notes

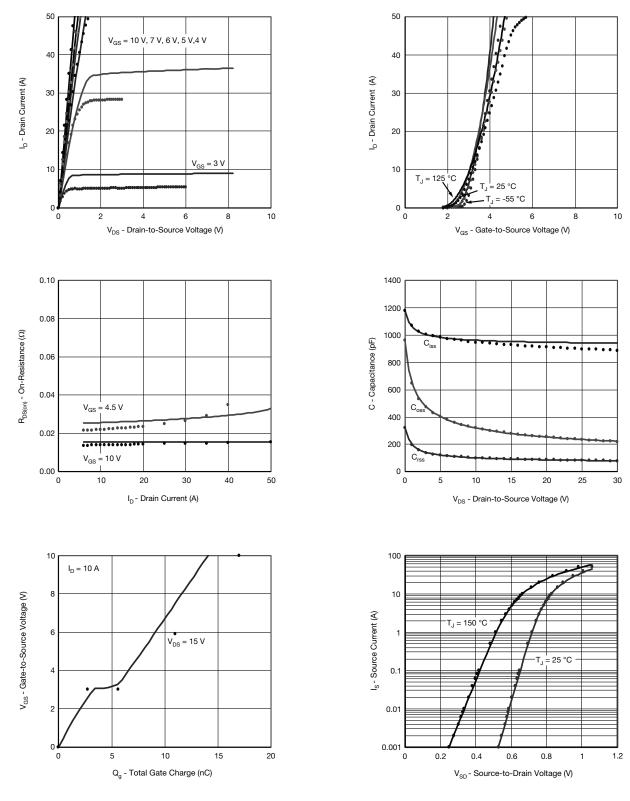
a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.



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COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)



Note

• Dots and squares represent measured data. Copyright: Vishay Intertechnology, Inc.

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