

Vishay Siliconix

N-Channel 150 V (D-S) MOSFET

DESCRIPTION

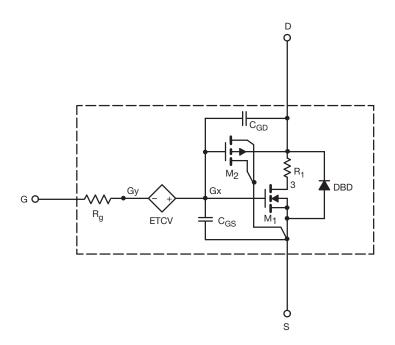
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over -55 °C to +125 °C temperature range
- · Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.





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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	3	-	V
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	0.0300	0.0285	Ω
		$V_{GS} = 7.5 \text{ V}, I_D = 10 \text{ A}$	0.0340	0.0315	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 10 A	17	18	S
Diode Forward Voltage	V_{SD}	I _S = 5 A	0.79	0.79	V
Dynamic ^b					
Input Capacitance	C _{iss}	$V_{DS} = 75 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	815	740	pF
Output Capacitance	Coss		175	145	
Reverse Transfer Capacitance	C _{rss}		19	8.5	
Total Gate Charge	Q_g	V _{DS} = 75 V, V _{GS} = 10 V, I _D = 10 A	13	14	- nC
		$V_{DS} = 75 \text{ V}, V_{GS} = 7.5 \text{ V}, I_{D} = 10 \text{ A}$	10	11	
Gate-Source Charge	Q_{gs}		3.7	3.7	
Gate-Drain Charge	Q_{gd}		3.9	3.9	

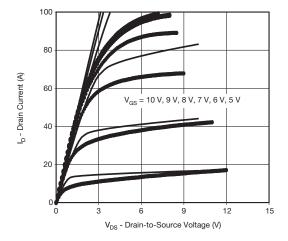
Notes

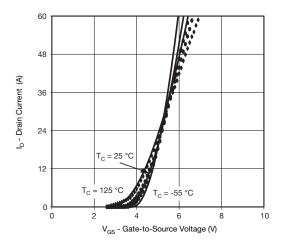
- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing

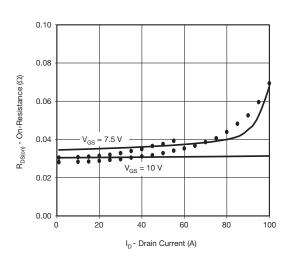
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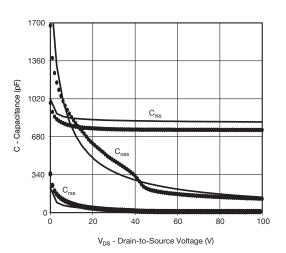
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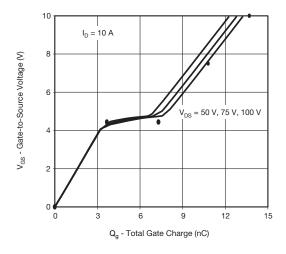
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)

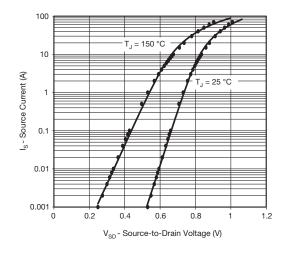












Note

• Dots and squares represent measured data.

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