

P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^e	Q_g (Typ.)
- 20	0.032 at $V_{GS} = - 4.5$ V	- 16	14.5 nC
	0.046 at $V_{GS} = - 2.5$ V	- 14.3	
	0.065 at $V_{GS} = - 2.0$ V	- 12	
	0.120 at $V_{GS} = - 1.8$ V	- 2.5	

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Ultra-small 1.5 mm x 1 mm Maximum Outline
- Ultra-thin 0.59 Maximum Height
- Compliant to RoHS Directive 2002/95/EC

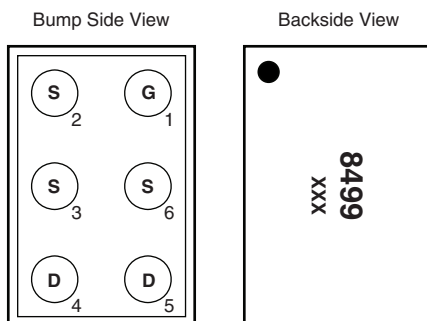


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

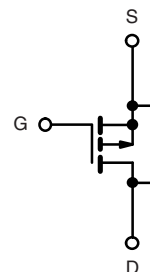
- Low On-Resistance Load Switch, Charger Switch and Battery Switch for Portable Devices
 - Low Power Consumption
 - Increased Battery Life

MICRO FOOT



Device Marking: 8499

xxx = Date/Lot Traceability Code



Ordering Information: Si8499DB-T2-E1 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$	A
		$T_C = 70^\circ\text{C}$	
		$T_A = 25^\circ\text{C}$	
		$T_A = 70^\circ\text{C}$	
Pulsed Drain Current	I_{DM}	- 20	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$	
		$T_A = 25^\circ\text{C}$	- 2.3 ^{a, b}
Maximum Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	W
		$T_C = 70^\circ\text{C}$	
		$T_A = 25^\circ\text{C}$	
		$T_A = 70^\circ\text{C}$	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$
Package Reflow Conditions ^c	IR/Convection	260	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. $t = 10$ s.

c. Refer to IPC/JEDEC (J-STD-020C), no manual or hand soldering.

d. Case is defined as the top surface of the package.

e. Based on $T_C = 25^\circ\text{C}$.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	R_{thJA}	37	45	°C/W
Maximum Junction-to-Case (Drain)	Steady State R_{thJC}	7	9.5	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. Maximum under Steady State conditions is 85 °C/W.

c. Case is defined as top surface of the package.

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	- 20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		- 20		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.2		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 0.5		- 1.3	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$			- 1	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 70\text{ }^{\circ}\text{C}$			- 10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	- 5			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -1.5\text{ A}$		0.026	0.032	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -1.5\text{ A}$		0.036	0.046	
		$V_{GS} = -2.0\text{ V}, I_D = -1\text{ A}$		0.048	0.065	
		$V_{GS} = -1.8\text{ V}, I_D = -0.5\text{ A}$		0.060	0.120	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -1.5\text{ A}$		10		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1300		pF
Output Capacitance	C_{oss}			250		
Reverse Transfer Capacitance	C_{rss}			200		
Total Gate Charge	Q_g	$V_{DS} = -10\text{ V}, V_{GS} = -5\text{ V}, I_D = -1.5\text{ A}$		20	30	nC
Gate-Source Charge	Q_{gs}	$V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -1.5\text{ A}$		14.5	22	
Gate-Drain Charge	Q_{gd}			2.0		
Gate Resistance	R_g	$V_{GS} = -0.1\text{ V}, f = 1\text{ MHz}$		4.1		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 6.7\text{ }\Omega$ $I_D \cong -1.5\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		7	15	ns
Rise Time	t_r			20	40	
Turn-Off Delay Time	$t_{d(off)}$			25	50	
Fall Time	t_f			50	100	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 6.7\text{ }\Omega$ $I_D \cong -1.5\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		30	60	
Rise Time	t_r			7	15	
Turn-Off Delay Time	$t_{d(off)}$			10	20	
Fall Time	t_f			55	110	
				30	60	

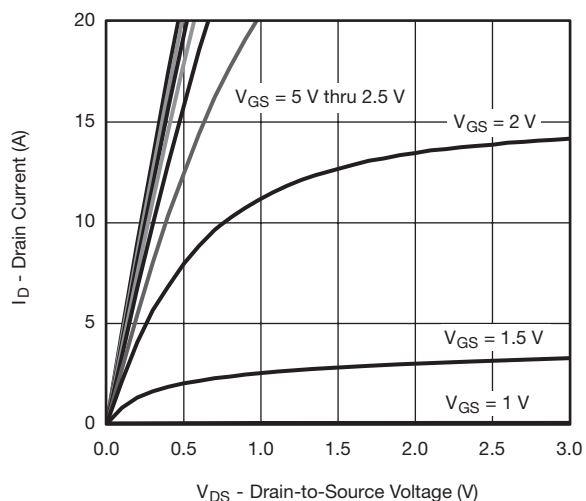
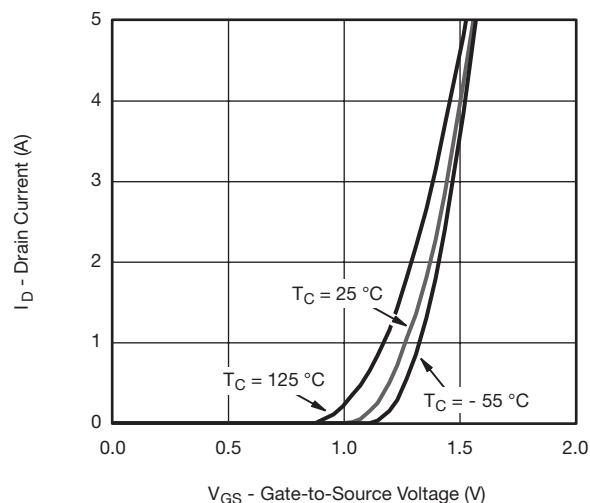
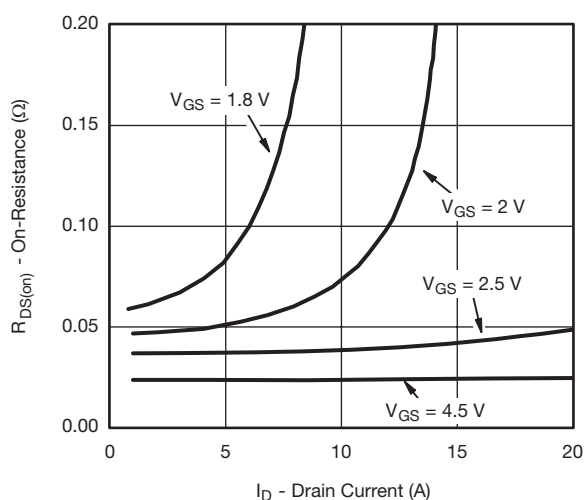
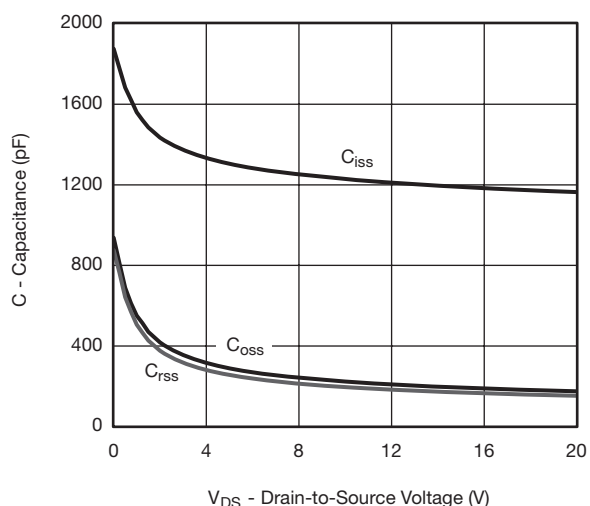
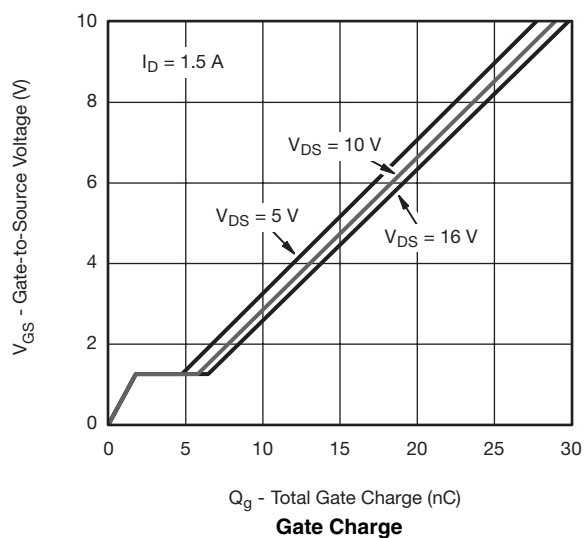
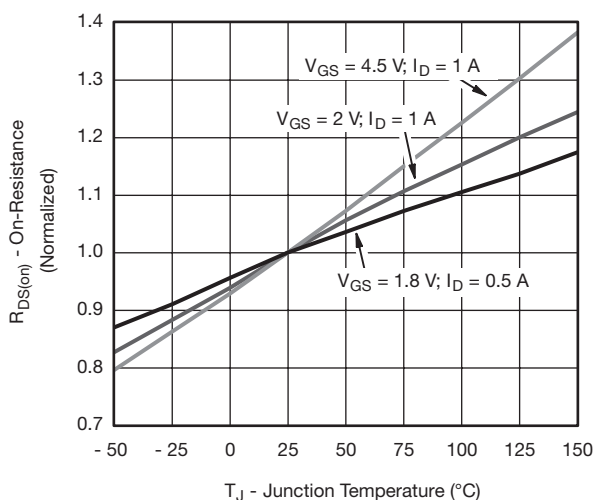


SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$			- 10.8	A
Pulse Diode Forward Current	I_{SM}				- 20	
Body Diode Voltage	V_{SD}	$I_S = -1.5\text{ A}$, $V_{GS} = 0\text{ V}$		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -1.5\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$		40	80	ns
Body Diode Reverse Recovery Charge	Q_{rr}			22	45	nC
Reverse Recovery Fall Time	t_a			15		ns
Reverse Recovery Rise Time	t_b			25		

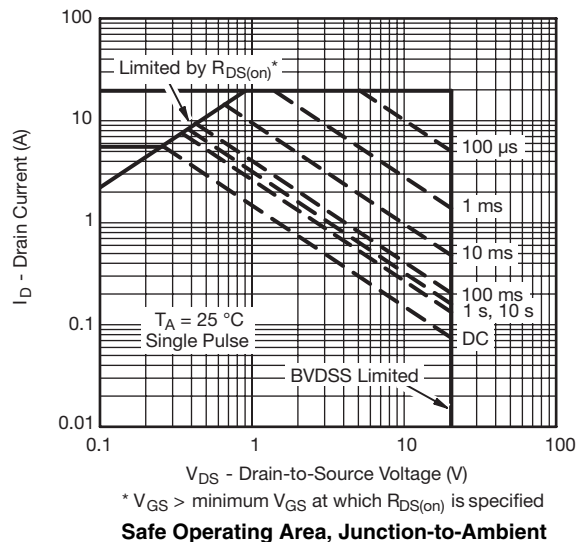
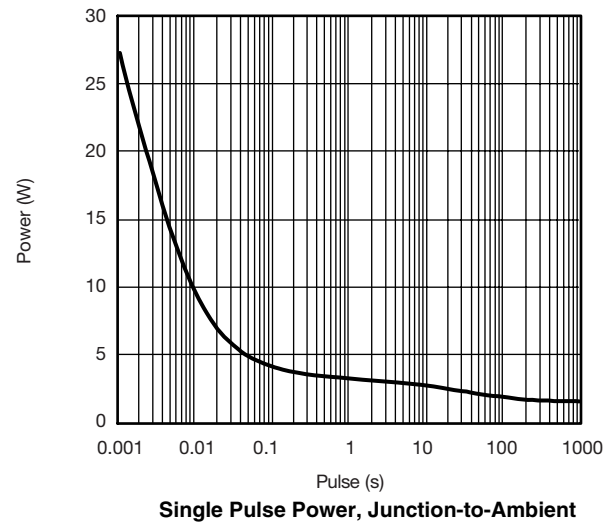
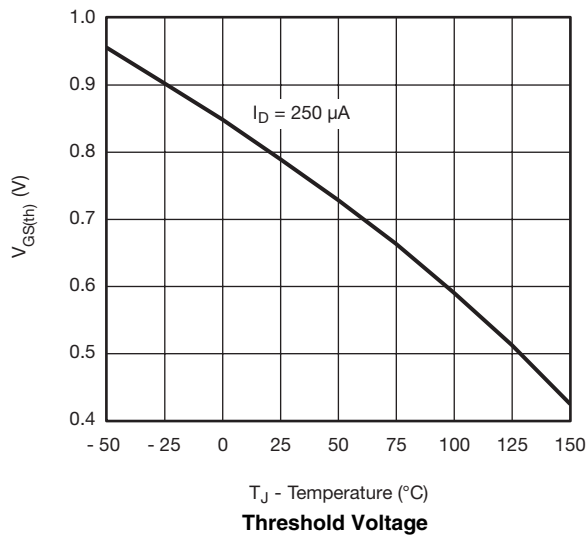
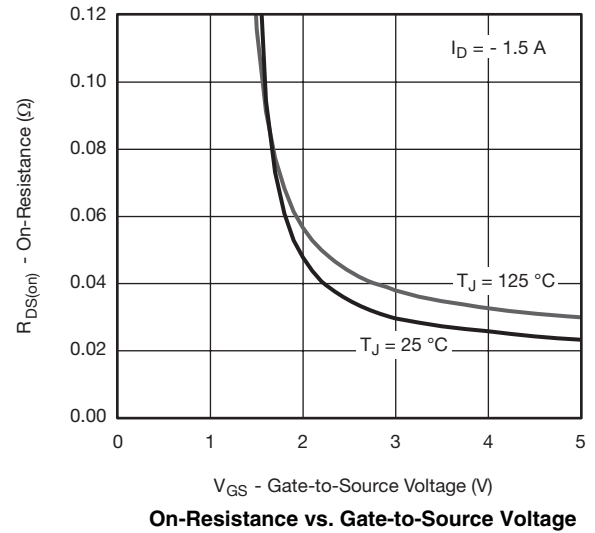
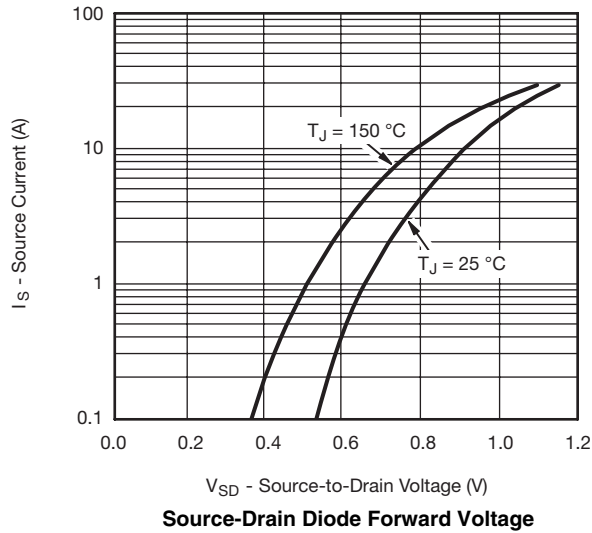
Notes:

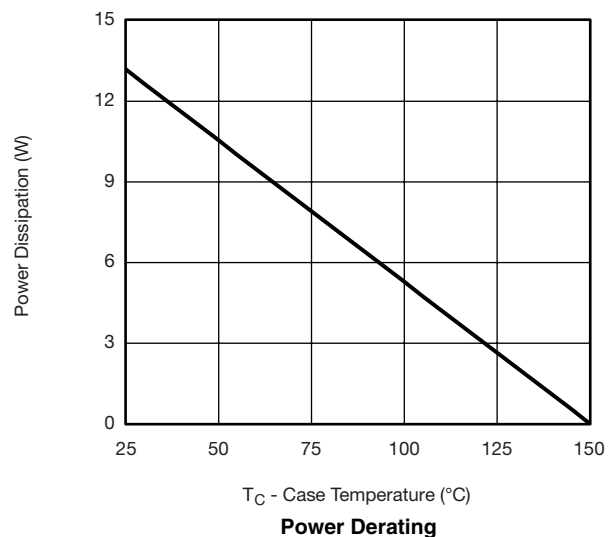
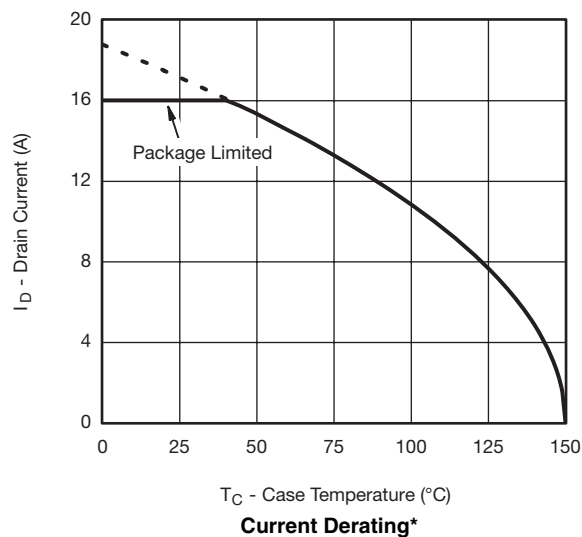
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

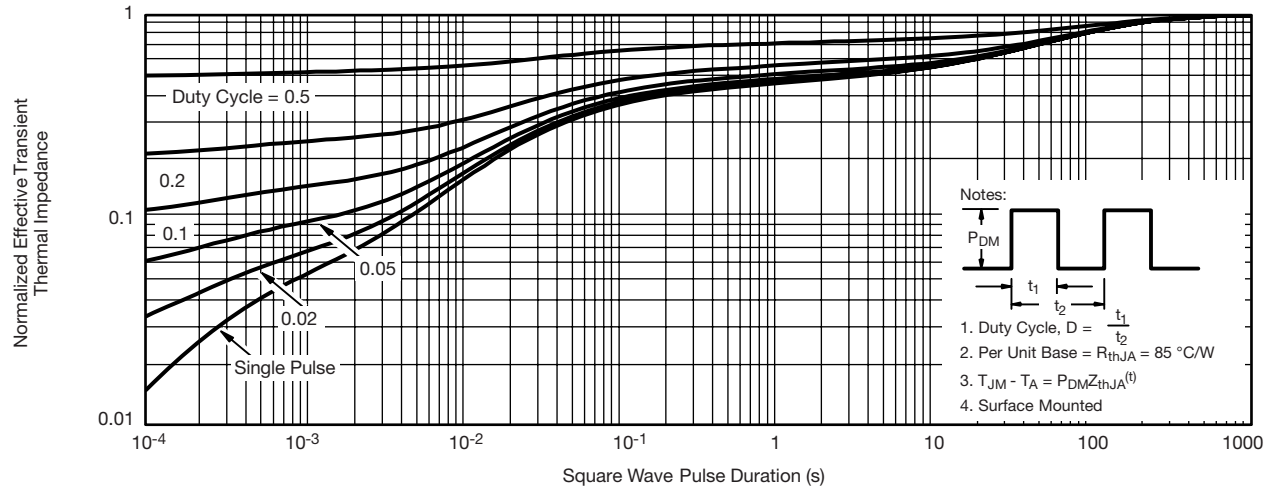
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



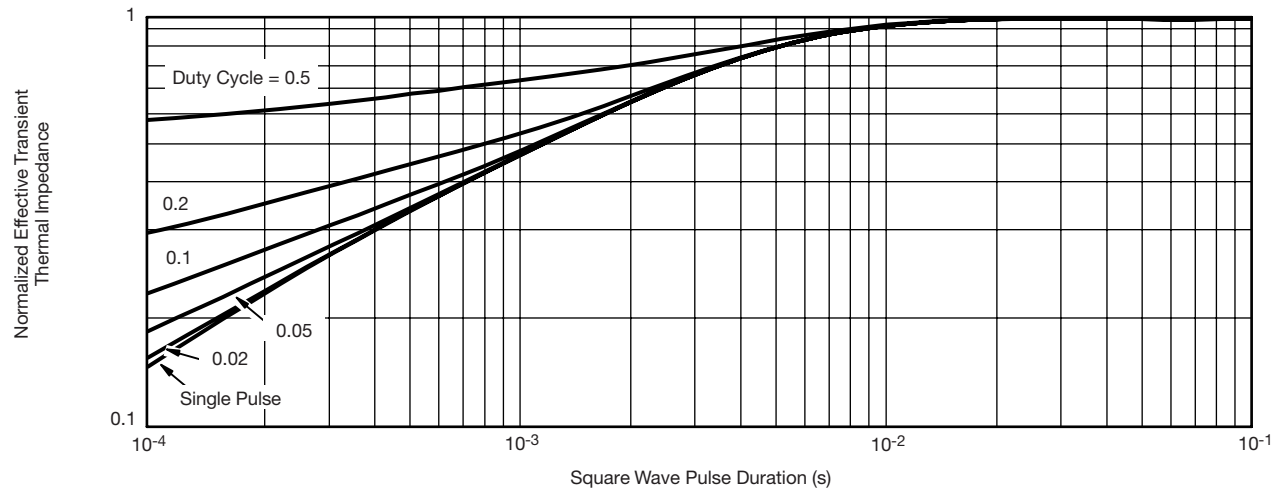
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

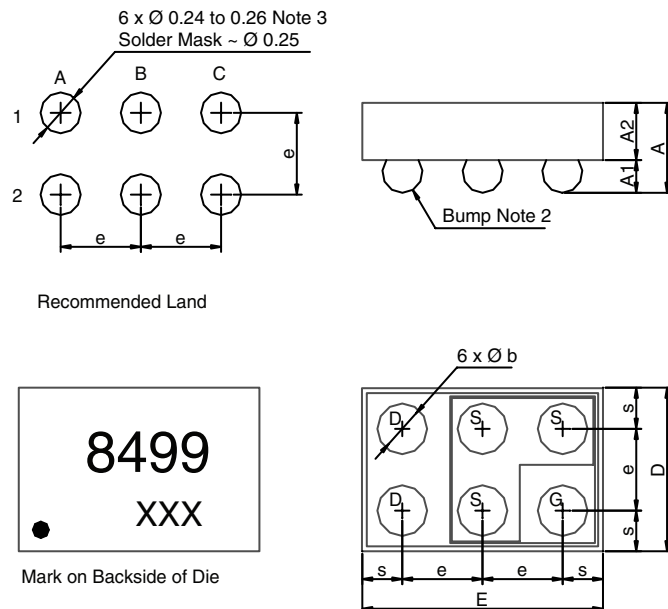
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

PACKAGE OUTLINE**MICRO FOOT: 6-BUMP (2 x 3, 0.5 mm PITCH)**

Notes (Unless Otherwise Specified):

1. All dimensions are in millimeters.
2. Six (6) solder bumps are lead (Pb)-free 95.5Sn, 3.8Ag, 0.7Cu with diameter $\varnothing 0.30$ to 0.32 mm.
3. Backside surface is coated with a Ti/Ni/Ag layer.
4. Non-solder mask defined copper landing pad.
5. • is location of Pin 1.

Dim.	Millimeters ^a			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.510	0.575	0.590	0.0201	0.0224	0.0232
A₁	0.220	0.250	0.280	0.0087	0.0098	0.0110
A₂	0.290	0.300	0.310	0.0114	0.0118	0.0122
b	0.300	0.310	0.320	0.0118	0.0122	0.0126
e	0.500			0.0197		
s	0.230	0.250	0.270	0.0090	0.0098	0.0106
D	0.920	0.960	1.000	0.0362	0.0378	0.0394
E	1.420	1.460	1.500	0.0559	0.0575	0.0591

Notes:

- a. Use millimeters as the primary measurement.

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