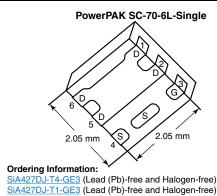




P-Channel 8 V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ.)	
- 8	0.016 at V _{GS} = - 4.5 V	- 12 ^a		
	0.0215 at V _{GS} = - 2.5 V	- 12 ^a		
	0.026 at V _{GS} = - 1.8 V	- 12 ^a	30 nC	
	0.032 at V _{GS} = - 1.5 V	- 12 ^a		
	0.095 at V _{GS} = - 1.2 V	- 3		



FEATURES

- TrenchFET[®] Power MOSFET
- New Thermally Enhanced PowerPAK[®] SC-70 Package
 - Small Footprint Area
 - Low On-Resistance
- 100 % R_g Tested
- Material categorization:

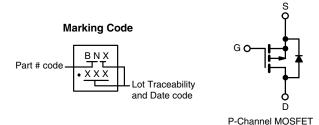
For definitions of compliance please see www.vishav.com/doc?99912



ROHS COMPLIANT HALOGEN FREE

APPLICATIONS

 Load Switch, for 1.2 V Power Line for Portable and Handheld Devices



Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	- 8	V	
Gate-Source Voltage		V_{GS}	± 5		
	T _C = 25 °C		- 12 ^a		
Continuous Drain Current /T 150 °C)	T _C = 70 °C	,	- 12 ^a		
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	I _D	- 12 ^{a, b, c}	А	
	T _A = 70 °C		- 9.9 ^{b, c}		
Pulsed Drain Current		I _{DM}	- 50		
Continuous Source-Drain Diode Current	T _C = 25 °C	,	- 12 ^a		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	- 2.9 ^{b, c}		
	T _C = 25 °C		19		
Maximum Power Dissipation	T _C = 70 °C		12	W	
	T _A = 25 °C	P _D	3.5 ^{b, c}	VV	
	T _A = 70 °C		2.2 ^{b, c}		
Operating Junction and Storage Temperature Ra	T _J , T _{stg}	- 55 to 150	°C		
Soldering Recommendations (Peak Temperature	_	260			

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	28	36	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	5.3	6.5	C/VV	

Notes:

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board.
- c t 5 s
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under steady state conditions is 80 °C/W.

Document Number: 66711 S12-1141-Rev. C, 21-May-12 For more information please contact: pmostechsupport@vishay.com

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	'			•	•		
Drain-Source Breakdown Voltage	V_{DS}	V _{GS} = 0, I _D = - 250 μA	- 8			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 050 A		- 5.8		m\//°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = - 250 μA		2.4		mV/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 0.35		- 0.8	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 5 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 8 V, V _{GS} = 0 V			- 1	μА	
		V_{DS} = -8 V, V_{GS} = 0 V, T_{J} = 55 °C			- 10		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le$ - 5 V, $V_{GS} =$ - 4.5 V	- 10			Α	
	ì	$V_{GS} = -4.5 \text{ V}, I_D = -8.2 \text{ A}$		0.013	0.016		
		$V_{GS} = -2.5 \text{ V}, I_D = -7.2 \text{ A}$		0.018	0.0215	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = -1.8 \text{ V}, I_D = -6.6 \text{ A}$		0.021	0.026		
		V _{GS} = - 1.5 V, I _D = - 1 A		0.025	0.032		
		V _{GS} = - 1.2 V, I _D = - 1 A		0.037	0.095		
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 4 V, I _D = - 8.2 A		37		S	
Dynamic ^b							
Input Capacitance	C _{iss}			2300		pF	
Output Capacitance	C _{oss}	$V_{DS} = -4 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		735			
Reverse Transfer Capacitance	C _{rss}			690			
Tatal Cata Chausa	0	V _{DS} = - 4 V, V _{GS} = - 5 V, I _D = - 10 A	33		50		
Total Gate Charge	Qg			30	45	nC	
Gate-Source Charge	Q_{gs}	$V_{DS} = -4 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -10 \text{ A}$		3			
Gate-Drain Charge	Q_{gd}			6.6			
Gate Resistance	R_{g}	f = 1 MHz	2	9	18	Ω	
Turn-On Delay Time	t _{d(on)}			20	30		
Rise Time	t _r	$V_{DD} = -4 \text{ V}, R_{L} = 0.4 \Omega$		20	30	ns	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ - 9.8 Å, V_{GEN} = - 4.5 V, R_g = 1 Ω		70	105		
Fall Time	t _f			40	60		
Drain-Source Body Diode Characteris	ics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 12	Δ	
Pulse Diode Forward Current	I _{SM}				- 50	_ A	
Body Diode Voltage	V_{SD}	I _S = - 9.8 A, V _{GS} = 0		- 0.8	- 1.2	٧	
Body Diode Reverse Recovery Time	t _{rr}			40	80	ns	
Body Diode Reverse Recovery Charge	irge O			12	25	nC	
Reverse Recovery Fall Time	t _a	$I_F = -9.8 \text{ A, dI/dt} = 100 \text{ A/}\mu\text{s, T}_J = 25 ^{\circ}\text{C}$		14			
Reverse Recovery Rise Time	t _b			26		ns	

Notes:

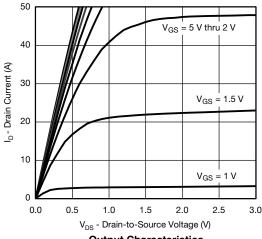
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

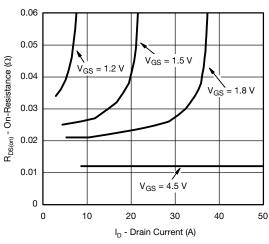


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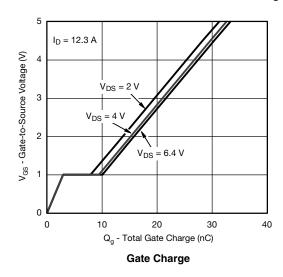
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

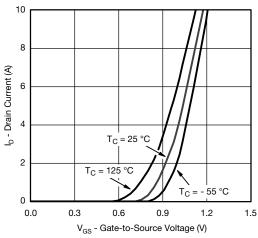


Output Characteristics

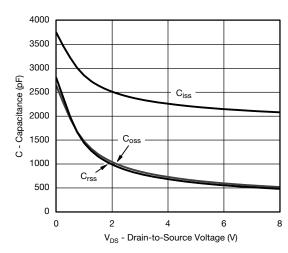


On-Resistance vs. Drain Current and Gate Voltage

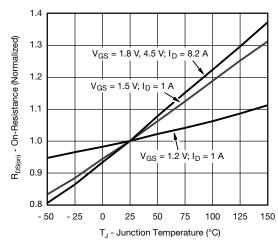




Transfer Characteristics



Capacitance



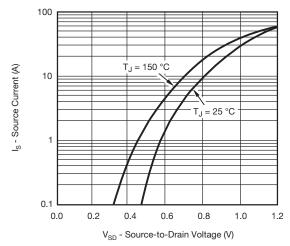
On-Resistance vs. Junction Temperature

0.06

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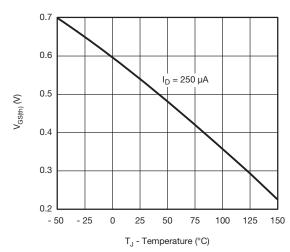
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

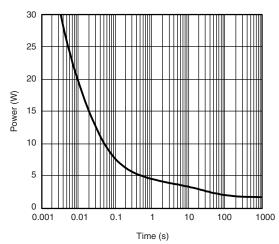


0.05 On-Resistance (Ω) 0.04 0.03 0.02 I_D = 1 A; T_J = 25 °C 0.01 0 0 3 4 5

Soure-Drain Diode Forward Voltage

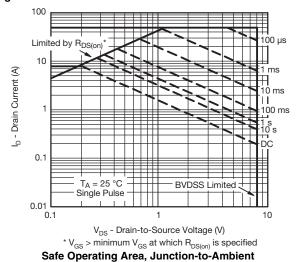
V_{GS} - Gate-to-Source Voltage (V) On-Resistance vs. Gate-to-Source Voltage





Threshold Voltage

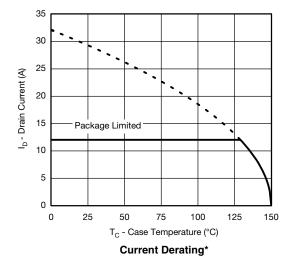
Single Pulse Power, Junction-to-Ambient

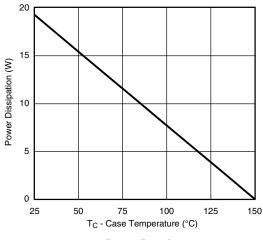




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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





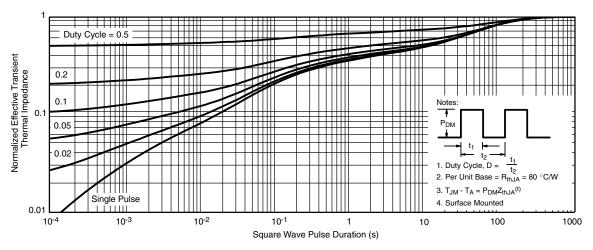
Power Derating

 $^{^{\}star}$ The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

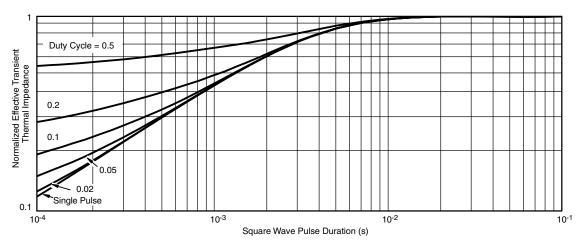
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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