## **SQ2351ES**

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**Vishay Siliconix** 

## Automotive P-Channel 20 V (D-S) 175 °C MOSFET



#### **FEATURES**

- TrenchFET<sup>®</sup> power MOSFET
- AEC-Q101 qualified <sup>d</sup>
- 100 %  $R_q$  and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

GO

P-Channel MOSFET

S

D



Marking Code: 8S

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	-20		
$R_{DS(on)} (\Omega)$ at $V_{GS} = -4.5 \text{ V}$	0.115		
$R_{DS(on)} (\Omega)$ at $V_{GS} = -2.5 V$	0.205		
I <sub>D</sub> (A)	-3.2		
Configuration	Single		

#### \_\_\_\_

ORDERING INFORMATION	
Package	SOT-23
Lead (Pb)-free and halogen-free	SQ2351ES (for detailed order number please see <u>www.vishay.com/doc?79771</u> )

ABSOLUTE MAXIMUM RATIN	<b>GS</b> (T <sub>C</sub> = 25 °C, unless	s otherwise noted	ł)	
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V <sub>DS</sub>	-20	V
Gate-source voltage		V <sub>GS</sub>	± 12	
Continuous drain current	T <sub>C</sub> = 25 °C	I	-3.2	
	T <sub>C</sub> = 125 °C	I <sub>D</sub>	-1.8	
Continuous source current (diode conduction) a		I <sub>S</sub>	-2.5	А
Pulsed drain current <sup>b</sup>		I <sub>DM</sub>	-12.7	
Single pulse avalanche current	L = 0.1 mH	I <sub>AS</sub>	-6	
Single pulse avalanche energy		E <sub>AS</sub>	1.8	mJ
Maximum power dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	D	2	W
	T <sub>C</sub> = 125 °C	P <sub>D</sub>	0.67	vv
Operating junction and storage temperature	e range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount <sup>c</sup>	R <sub>thJA</sub>	175	°C/W
Junction-to-foot (drain)		R <sub>thJF</sub>	75	0/10

#### Notes

- a. Package limited
- b. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %
- c. When mounted on 1" square PCB (FR4 material)
- d. Parametric verification ongoing

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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static	•				1	<u> </u>	
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub>	= 0, I <sub>D</sub> = -250 μΑ	-20	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-0.6	-1.0	-1.5	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	0 V, $V_{GS} = \pm 12 V$	-	-	± 100	nA
		$V_{GS} = 0 V$	V <sub>DS</sub> = -20 V	-	-	-1	
Zero gate voltage drain current	I <sub>DSS</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = -20 V, T <sub>J</sub> = 125 °C	-	-	-50	μA
		$V_{GS} = 0 V$	V <sub>DS</sub> = -20 V, T <sub>J</sub> = 175 °C	-	-	-150	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{GS} = -4.5 V$	$V_{DS} \ge 5 V$	-8	-	-	Α
Drain-source on-state resistance <sup>a</sup>		V <sub>GS</sub> = -4.5 V	I <sub>D</sub> = -2.4 A	-	0.080	0.115	Ω
		V <sub>GS</sub> = -4.5 V	I <sub>D</sub> = -2.4 A, T <sub>J</sub> = 125 °C	-	-	0.168	
	R <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V	I <sub>D</sub> = -2.4 A, T <sub>J</sub> = 175 °C	-	-	0.196	
		V <sub>GS</sub> = -2.5 V	I <sub>D</sub> = -1.8 A	-	0.150	0.205	
Forward transconductance b	9 <sub>fs</sub>	V <sub>DS</sub> =	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -2.4 A		6	-	S
Dynamic <sup>b</sup>	•	•			•	•	
Input capacitance	C <sub>iss</sub>			-	265	330	
Output capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = -10 V, f = 1 MHz	-	75	94	pF
Reverse transfer capacitance	C <sub>rss</sub>			-	50	63	
Total gate charge <sup>c</sup>	Qg			-	3.4	5.5	
Gate-source charge c	Q <sub>gs</sub>	V <sub>GS</sub> = -4.5 V	$V_{DS} = -10 \text{ V}, \text{ I}_{D} = -2.4 \text{ A}$	-	0.6	-	nC
Gate-drain charge c	Q <sub>gd</sub>			-	1.1	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz		2.8	9.6	14.4	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>			-	20	30	
Rise time <sup>c</sup>	t <sub>r</sub>	$V_{DD}$ = -10 V, R <sub>L</sub> = 5.21 $\Omega$ I <sub>D</sub> $\cong$ -1.9 A, V <sub>GEN</sub> = -4.5 V, R <sub>g</sub> = 1 $\Omega$		-	18	27	ns
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	19	28	
Fall time <sup>c</sup>	t <sub>f</sub>			-	8	12	
Source-Drain Diode Ratings and Char	racteristics						
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	-12.7	Α
Forward voltage	V <sub>SD</sub>	$I_{\rm F} = -2$ A, $V_{\rm GS} = 0$		_	-0.8	-1.2	V

Notes

a. Pulse test; pulse width  $\leq 300~\mu\text{s},~\text{duty}~\text{cycle} \leq 2~\%$ 

b. Guaranteed by design, not subject to production testing

c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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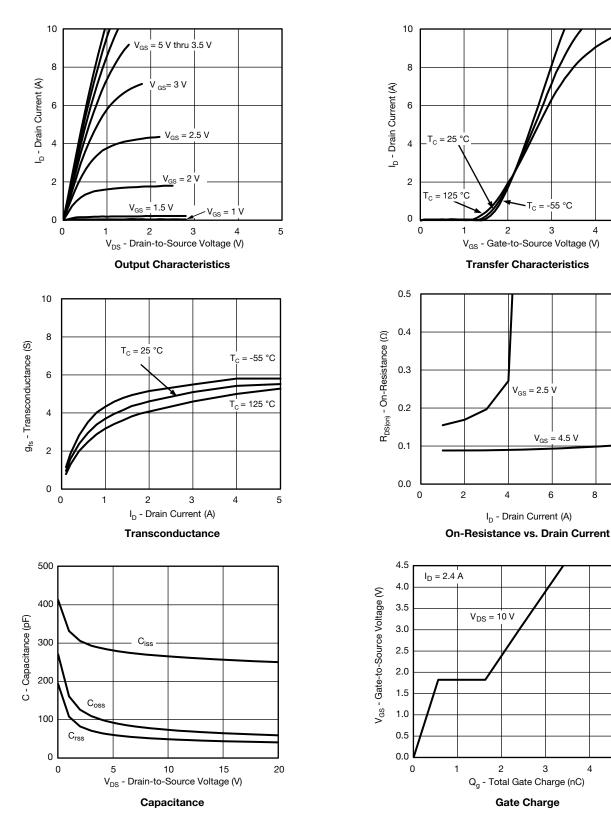
4

8

10

5

### **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



3

5

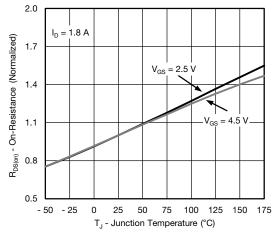
4

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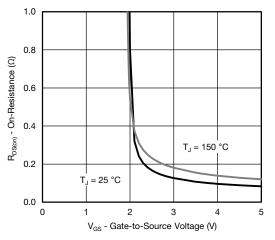


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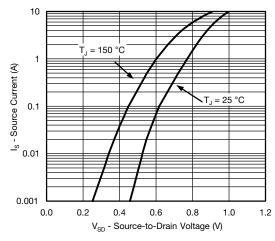
### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



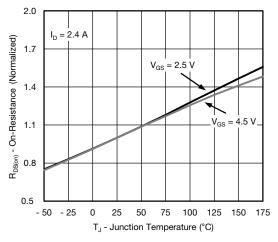
On-Resistance vs. Junction Temperature (1.8 A)



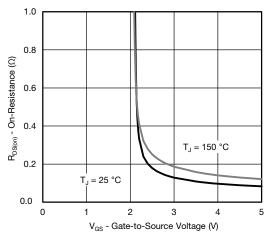
On-Resistance vs. Gate-to-Source Voltage (1.8 A)



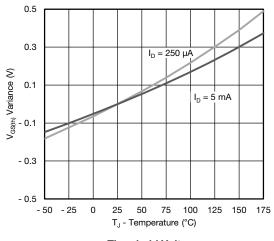
Source-Drain Diode Forward Voltage



On-Resistance vs. Junction Temperature (2.4 A)



On-Resistance vs. Gate-to-Source Voltage (2.4 A)



**Threshold Voltage** 

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0.1

0.01 10-4

0.05

0.02

Single Pulse

10<sup>-3</sup>

10-2

10-1

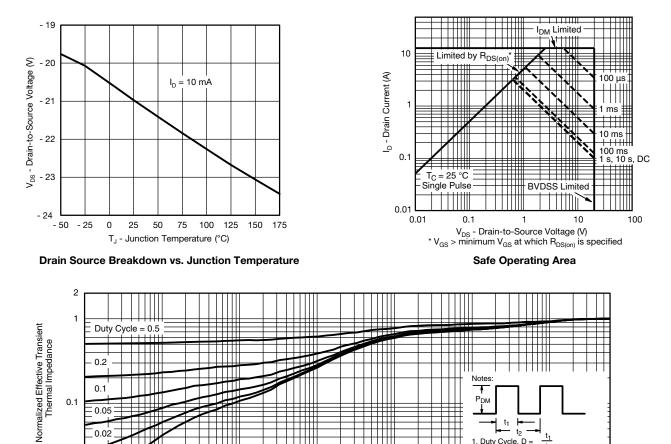
Square Wave Pulse Duration (s) Normalized Thermal Transient Impedance, Junction-to-Ambient

1

ТĨШ

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#### **THERMAL RATINGS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



PDN

10

t1

1. Duty Cycle, D =

4. Surface Mounted

t2

2. Per Unit Base = RthJA

3.  $T_{JM} - T_A = P_{DM}Z_{thJA}^{(t)}$ 

t<sub>1</sub>

t<sub>2</sub>

100

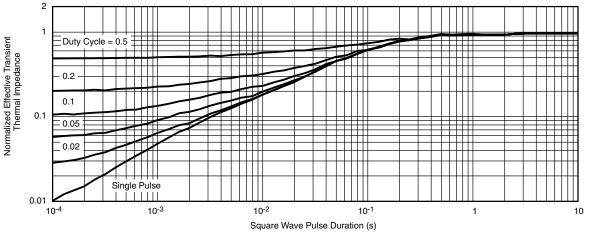
= 175 °C/W



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#### THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Foot

#### Note

The characteristics shown in the two graphs

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- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
- Normalized Transient Thermal Impedance Junction-to-Foot (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?66716.



# Package Information

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### SOT-23 (TO-236): 3-LEAD







Dim	MILLIN	METERS	INCHES		
	Min	Max	Min	Мах	
Α	0.89	1.12	0.035	0.044	
A <sub>1</sub>	0.01	0.10	0.0004	0.004	
A <sub>2</sub>	0.88	1.02	0.0346	0.040	
b	0.35	0.50	0.014	0.020	
С	0.085	0.18	0.003	0.007	
D	2.80	3.04	0.110	0.120	
E	2.10	2.64	0.083	0.104	
E <sub>1</sub>	1.20	1.40	0.047	0.055	
е	0.95 BSC		0.0374 Ref		
e <sub>1</sub>	1.90 BSC		0.0748 Ref		
L	0.40	0.60	0.016	0.024	
L <sub>1</sub>	0.64 Ref		0.025 Ref		
S	0.50 Ref		0.020 Ref		
q	3°	8°	3°	8°	



# Application Note 826

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#### **RECOMMENDED MINIMUM PADS FOR SOT-23**



Recommended Minimum Pads Dimensions in Inches/(mm)

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