

N-Channel 200 V (D-S) 175 °C MOSFET

DESCRIPTION

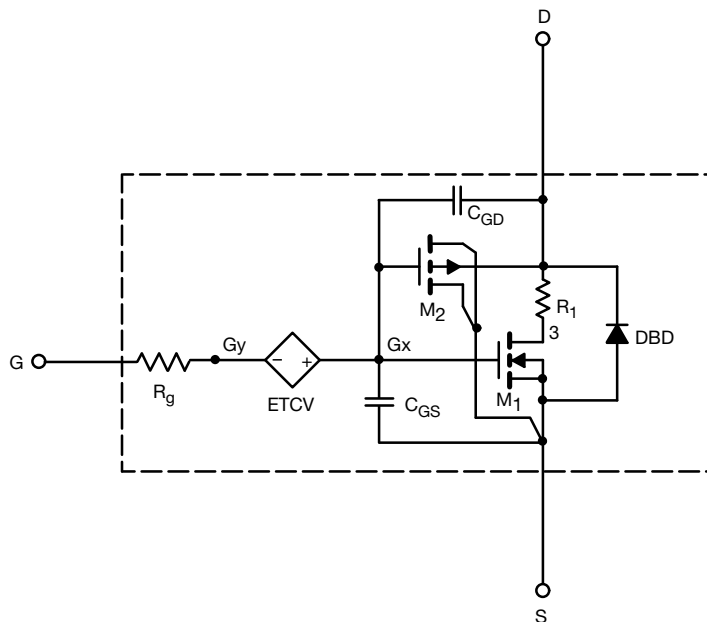
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over -55 °C to +125 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



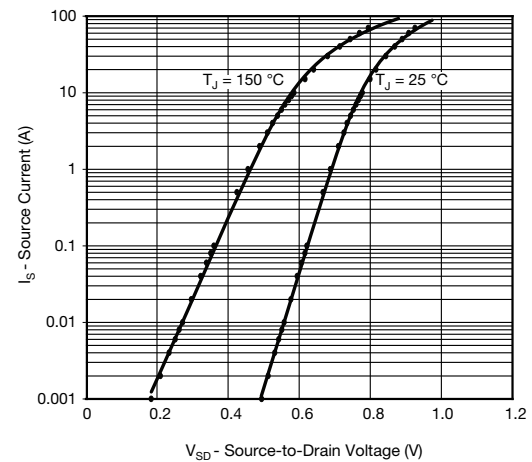
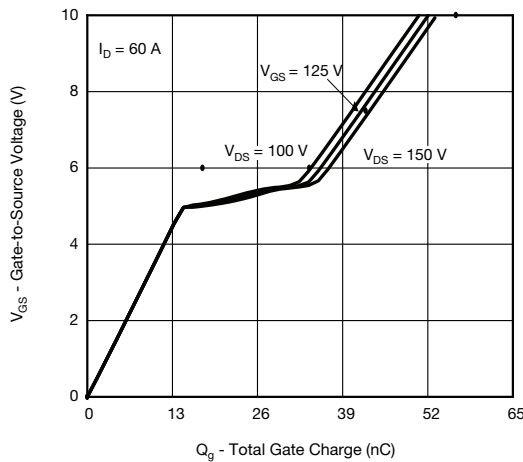
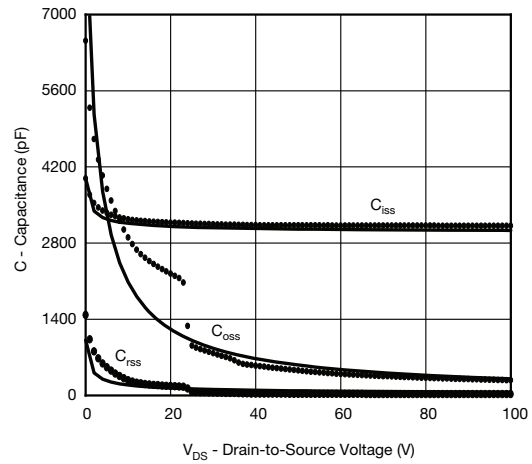
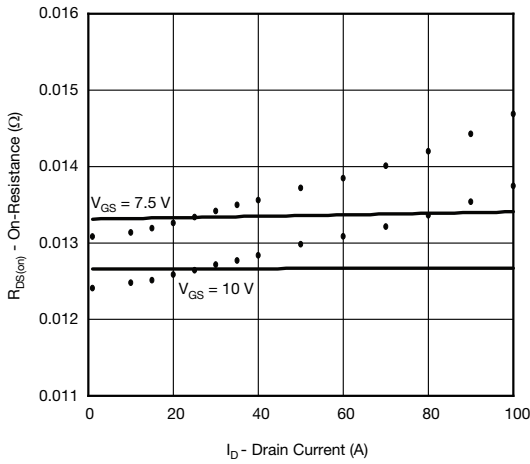
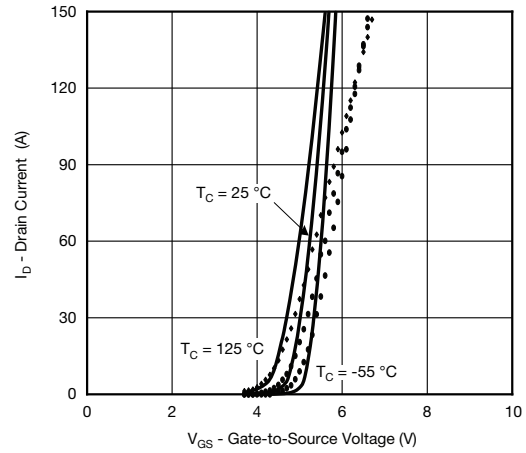
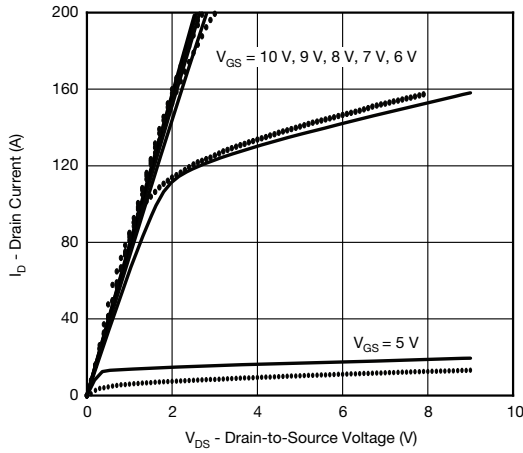
| SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | |
|--|--------------|--|----------------|---------------|----------|
| PARAMETER | SYMBOL | TEST CONDITIONS | SIMULATED DATA | MEASURED DATA | UNIT |
| Static | | | | | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | 3.5 | - | V |
| Drain-Source On-State Resistance ^a | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 30\text{ A}$ | 0.0126 | 0.0123 | Ω |
| | | $V_{GS} = 7.5\text{ V}, I_D = 30\text{ A}$ | 0.0133 | 0.0130 | |
| Forward Transconductance ^a | g_{fs} | $V_{DS} = 15\text{ V}, I_D = 30\text{ A}$ | 98 | 63 | S |
| Diode Forward Voltage | V_{SD} | $I_S = 30\text{ A}$ | 0.84 | 0.85 | V |
| Dynamic ^b | | | | | |
| Input Capacitance | C_{iss} | $V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ | 3030 | 3120 | pF |
| Output Capacitance | C_{oss} | | 305 | 280 | |
| Reverse Transfer Capacitance | C_{rss} | | 60 | 24 | |
| Total Gate Charge | Q_g | $V_{DS} = 100\text{ V}, V_{GS} = 10\text{ V}, I_D = 60\text{ A}$ | 54 | 58 | nC |
| Gate-Source Charge | Q_{gs} | | 17.6 | 17.6 | |
| Gate-Drain Charge | Q_{gd} | | 17.2 | 17.2 | |

Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

- Dots and squares represent measured data.

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