### **SPICE Device Model SiR864DP**



Vishay Siliconix

### N-Channel 30 V (D-S) MOSFET

### DESCRIPTION

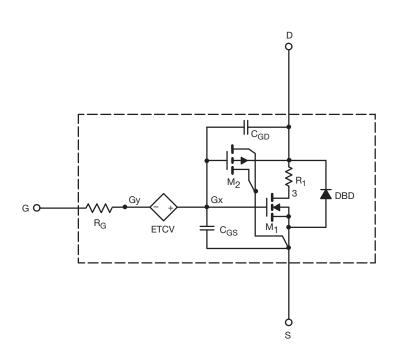
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### SUBCIRCUIT MODEL SCHEMATIC

### **CHARACTERISTICS**

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the 55 °C to + 125 °C Temperature Range
- Model the Gate Charge



#### Note

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

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<b>SPECIFICATIONS</b> $T_J = 25 \text{ °C}$ , unless otherwise noted					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \ \mu A$	1.3	-	V
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 15 \text{ A}$	0.0029	0.0030	Ω
		$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 10 \text{ A}$	0.0036	0.0036	
Forward Transconductance <sup>a</sup>	<b>g</b> fs	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 15 \text{ A}$	67	75	S
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 5 A	0.71	0.71	V
Dynamic <sup>b</sup>					
Input Capacitance	C <sub>iss</sub>	$V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1 MHz	2390	2460	pF
Output Capacitance	C <sub>oss</sub>		561	550	
Reverse Transfer Capacitance	C <sub>rss</sub>		198	200	
Total Gate Charge	Qg	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	38	43	nC
			19	20	
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS}$ = 15 V, $V_{GS}$ = 4.5 V, $I_{D}$ = 10 A	5.9	5.9	
Gate-Drain Charge	Q <sub>gd</sub>		5.8	5.8	

Notes

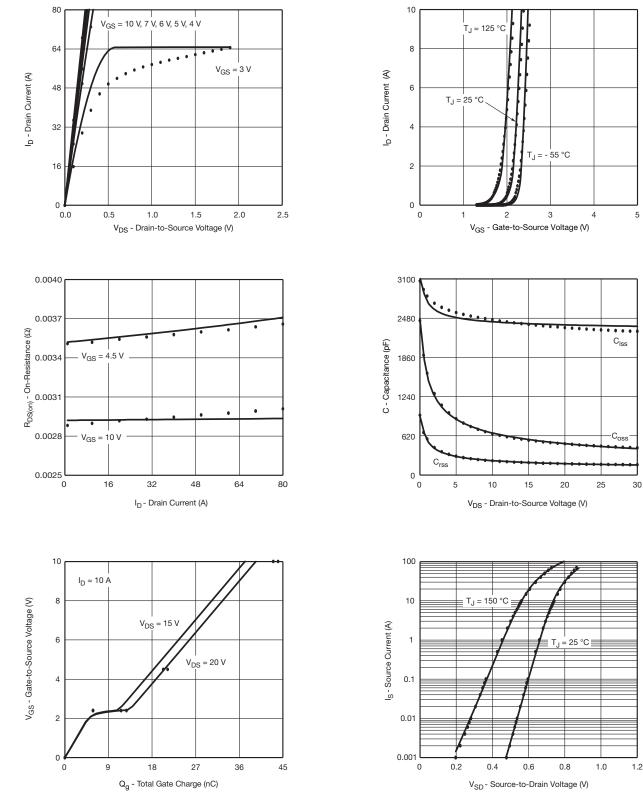
a. Pulse test; pulse width  $\leq 300~\mu\text{s},$  duty cycle  $\leq 2~\%.$ 

b. Guaranteed by design, not subject to production testing.



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### COMPARISON OF MODEL WITH MEASURED DATA $T_{\rm J}$ = 25 °C, unless otherwise noted



Note Dots and squares represent measured data.

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