

Vishay Siliconix

# Automotive N-Channel 20 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY								
V <sub>DS</sub> (V)	20							
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.028							
$R_{DS(on)}(\Omega)$ at $V_{GS} = 2.5 \text{ V}$	0.034							
$R_{DS(on)}(\Omega)$ at $V_{GS} = 1.8 \text{ V}$	0.038							
I <sub>D</sub> (A)	7.8							
Configuration	Single							

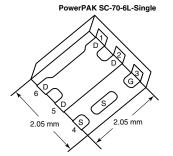
#### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- AEC-Q101 Qualified d
- 100 % R<sub>q</sub> and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

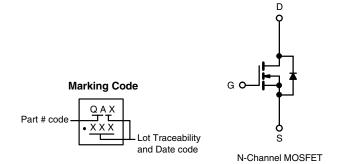




FREE



Ordering Information: SQA410EJ-T1-GE3 (Lead (Pb)-free and Halogen-free)



ORDERING INFORMATION						
Package	PowerPAK SC-70					
Lead (Pb)-free and Halogen-free	SQA410EJ-T1-GE3					

PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		V <sub>DS</sub>	20	V		
Gate-Source Voltage		V <sub>GS</sub>	20			
Continuous Drain Currenta	T <sub>C</sub> = 25 °C		7.8			
Continuous Drain Current	T <sub>C</sub> = 125 °C	I <sub>D</sub>	7.8			
Continuous Source Current (Diode Conduction	on) <sup>a</sup>	Is	7.8	Α		
Pulsed Drain Current <sup>a</sup>		I <sub>DM</sub>	24			
Single Pulse Avalanche Current	I _ 0.1 m∐	I <sub>AS</sub>	10			
Single Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	5	mJ		
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	В	13.6	W		
	T <sub>C</sub> = 125 °C	$P_{D}$	4.5	]		
Operating Junction and Storage Temperature	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C			
Soldering Recommendations (Peak Tempera		260	°C			

THERMAL RESISTANCE RATINGS								
PARAMETER		SYMBOL	LIMIT	UNIT				
Junction-to-Ambient	PCB Mount <sup>c</sup>	R <sub>thJA</sub>	90	°C/W				
Junction-to-Case (Drain)		$R_{thJC}$	11	G/VV				

## Notes

- a. Package limited.
- b. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.
- c. When mounted on 1" square PCB (FR-4 material).
- d. Parametric verification ongoing.
- e. See solder profile (<a href="www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



# Vishay Siliconix

PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static				,		ı		
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> =	20		-	W		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$			1.1	V	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA	
		$V_{GS} = 0 V$ $V_{DS} = 20 V$		-	-	1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = 20 V, T <sub>J</sub> = 125 °C	-	-	50	μA	
		$V_{GS} = 0 V$	V <sub>DS</sub> = 20 V, T <sub>J</sub> = 175 °C	-	-	250		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 4.5 V	$V_{DS} \ge 5 V$	10	-	-	Α	
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 5 A	-	0.023	0.028		
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 5 A, T <sub>J</sub> = 125 °C	-	-	0.042		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 5 A, T <sub>J</sub> = 175 °C	-		0.050	Ω	
		V <sub>GS</sub> = 2.5 V	I <sub>D</sub> = 4 A	-	0.026	0.034		
		V <sub>GS</sub> = 1.8 V	I <sub>D</sub> = 3 A	-	0.031	0.038		
Forward Transconductanceb	V <sub>DS</sub>	= 15 V, I <sub>D</sub> = 5 A	-	31	-	S		
Dynamic <sup>b</sup>								
Input Capacitance	C <sub>iss</sub>			-	388	485		
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V V <sub>DS</sub> = 10 V, f = 1 MHz		-	80	100	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	36	45	1	
Total Gate Charge <sup>c</sup>	Qg				5	8		
Gate-Source Charge <sup>c</sup>	$Q_{gs}$	$V_{GS} = 4.5 \text{ V}$ $V_{DS} = 10 \text{ V}, I_D = 5.1 \text{ A}$		-	0.55	-	nC	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$	1		-	0.79	-		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		6	11.89	18	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			-	8	12		
Rise Time <sup>c</sup>	t <sub>r</sub>	V <sub>DD</sub> :	-	8	12	ns		
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	I <sub>D</sub> ≅ 1 Å, \	-	21	32			
Fall Time <sup>c</sup>	t <sub>f</sub>			-	8	12		
Source-Drain Diode Ratings and Chara	acteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	24	Α	
Forward Voltage	V <sub>SD</sub>	$I_F = 4.5 \text{ A}, V_{GS} = 0 \text{ V}$			0.75	1.2	V	

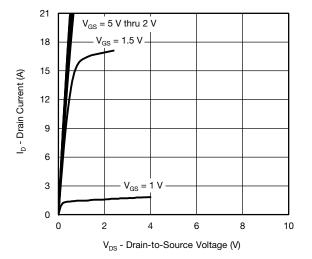
#### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

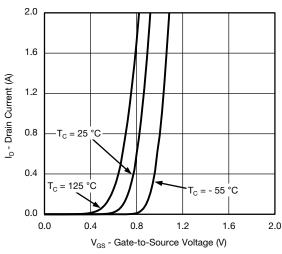
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



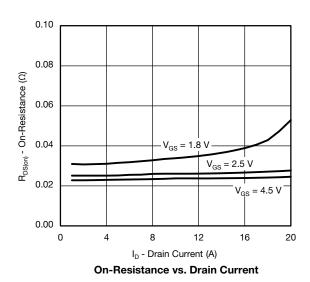
# **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



## **Output Characteristics**

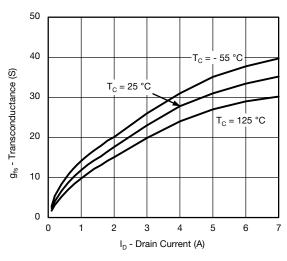


## Transfer Characteristics

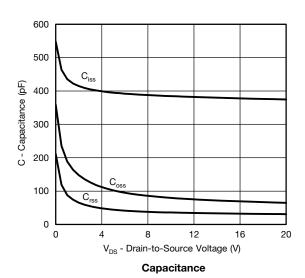


18 15 I<sub>D</sub> - Drain Current (A) 12 9  $T_C =$ 25 °C 6 125 3 - 55 °C 0 0 1.2 2.4 3 0.6 1.8 V<sub>GS</sub> - Gate-to-Source Voltage (V)

#### **Transfer Characteristics**

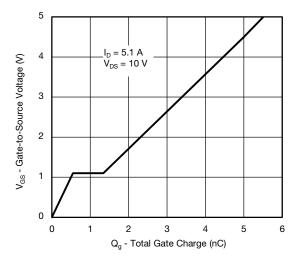


#### Transconductance

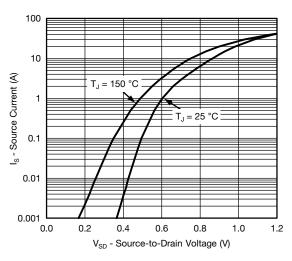




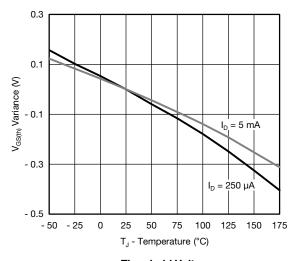
# **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



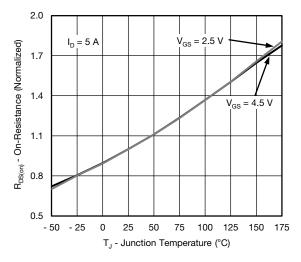
#### **Gate Charge**



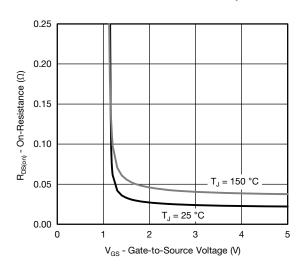
## **Source Drain Diode Forward Voltage**



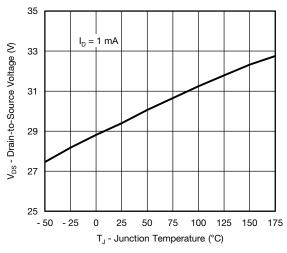
Threshold Voltage



#### On-Resistance vs. Junction Temperature



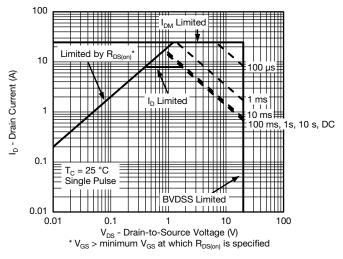
On-Resistance vs. Gate-to-Source Voltage



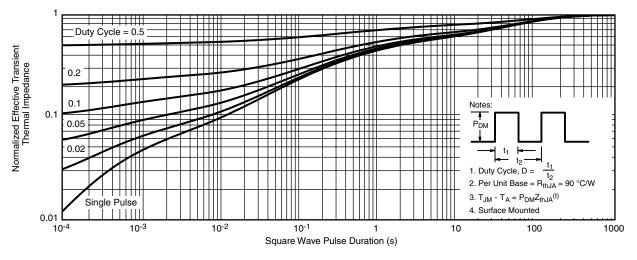
**Drain Source Breakdown vs. Junction Temperature** 



# **THERMAL RATINGS** ( $T_A = 25$ °C, unless otherwise noted)



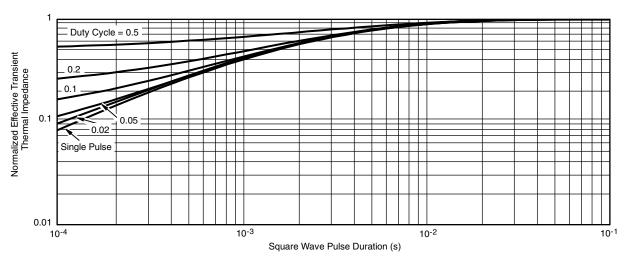
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



# THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



## Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?67072">www.vishay.com/ppg?67072</a>.





Vishay Siliconix

# PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
  Package outline exclusive of mold flash and metal burr
  Package outline inclusive of plating

	SINGLE PAD						DUAL PAD					
DIM	M	ILLIMETER	RS		INCHES		MILLIMETERS		RS		INCHES	
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
Е	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
е		0.65 BSC			0.026 BSC	;		0.65 BSC			0.026 BSC	
K		0.275 TYP			0.011 TYP		0.275 TYP			0.011 TYP		
K1		0.400 TYP		0.016 TYP		0.320 TYP			0.013 TYP			
K2		0.240 TYP		0.009 TYP		0.252 TYP			0.010 TYP			
К3		0.225 TYP		0.009 TYP						•	•	
K4		0.355 TYP		0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

ECN: C-07431 - Rev. C, 06-Aug-07

DWG: 5934

06-Aug-07



# RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

Return to Index

ATTLICATION NOT



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