Automotive P-Channel 30 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	- 30
$R_{DS(on)}$ (Ω) at V_{GS} = - 10 V	0.0085
$R_{DS(on)}$ (Ω) at V_{GS} = - 4.5 V	0.0200
I_D (A)	- 30[a]
Configuration	Single

FEATURES

- TrenchFET® Power MOSFET
- ESD Protection: 3000 V
- AEC-Q101 Qualified[d]
- 100 % R_g and UIS Tested
- Material categorization:
  For definitions of compliance please see www.vishay.com/doc?99912

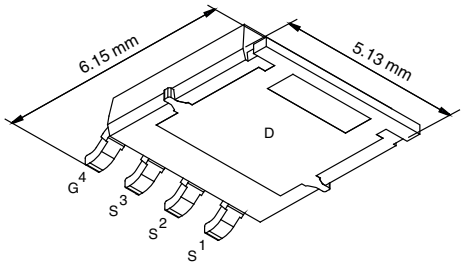
AUTOMOTIVE GRADE

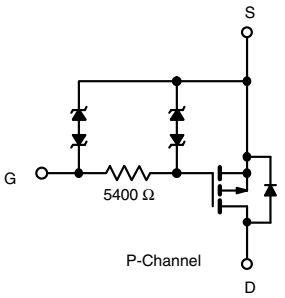
Pb-free

RoHS COMPLIANT

HALOGEN FREE

PowerPAK® SO-8L Single





ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and Halogen-free	SQJ403EEP-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	- 30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current[a]	T_C = 25 °C	I_D	- 30	A
	T_C = 125 °C		- 30	
Continuous Source Current (Diode Conduction)[a]		I_S	- 30	
Pulsed Drain Current[b]		I_{DM}	- 84	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	- 50	
Single Pulse Avalanche Energy		E_{AS}	125	mJ
Maximum Power Dissipation[b]	T_C = 25 °C	P_D	68	W
	T_C = 125 °C		22	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)[e, f]			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount[c]	R_{thJA}	68	°C/W
Junction-to-Case (Drain)		R_{thJC}	2.2	

Notes

a. Package limited.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
c. When mounted on 1" square PCB (FR-4 material).
d. Parametric verification ongoing.
e. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

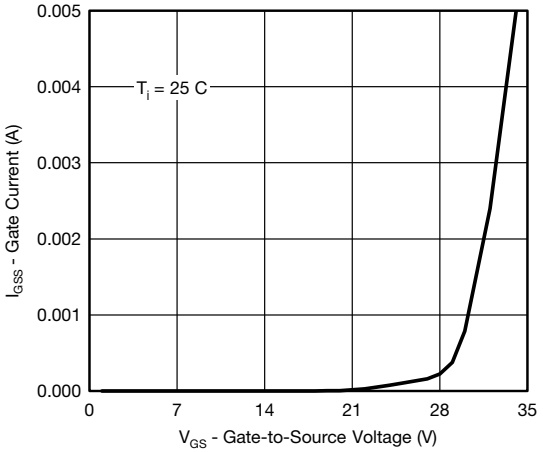
SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA		- 30	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA		- 1.5	- 2.0	- 2.5	
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V		-	-	± 2	µA
		V_{DS} = 0 V, V_{GS} = ± 20 V		-	-	± 1	mA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V	V_{DS} = - 30 V	-	-	- 1	µA
		V_{GS} = 0 V	V_{DS} = - 30V, T_J = 125 °C	-	-	- 50	
		V_{GS} = 0 V	V_{DS} = - 30V, T_J = 175 °C	-	-	- 250	
On-State Drain Current[a]	$I_{D(on)}$	V_{GS} = - 10 V	V_{DS} ≤ - 5 V	- 30	-	-	A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V	I_D = - 10 A	-	0.0070	0.0085	Ω
		V_{GS} = - 10 V	I_D = - 10 A, T_J = 125 °C	-	-	0.0130	
		V_{GS} = - 10 V	I_D = - 10 A, T_J = 175 °C	-	-	0.0150	
		V_{GS} = - 4.5 V	I_D = - 7 A	-	0.0120	0.0200	
Forward Transconductance[b]	g_{fs}	V_{DS} = - 10 V, I_D = - 10 A		-	32	-	S
Dynamic[b]							
Output Capacitance	C_{oss}	V_{GS} = 0 V	V_{DS} = - 15 V, f = 1 MHz	-	712	890	pF
Total Gate Charge[c]	Q_g	V_{GS} = - 10 V	V_{DS} = - 15 V, I_D = - 10 A	-	75	164	nC
Gate-Source Charge[c]	Q_{gs}			-	9.5	-	
Gate-Drain Charge[c]	Q_{gd}			-	19	-	
Gate Resistance	R_g	f = 1 MHz		2	4.3	7.5	kΩ
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = - 15 V, R_L = 1.5 Ω I_D ≅ - 10 A, V_{GEN} = - 10 V, R_g = 1 Ω		-	38	57	ns
Rise Time[c]	t_r			-	82	123	
Turn-Off Delay Time[c]	$t_{d(off)}$			-	134	201	
Fall Time[c]	t_f			-	178	214	
Source-Drain Diode Ratings and Characteristics[b]							
Pulsed Current[a]	I_{SM}			-	-	- 84	A
Forward Voltage	V_{SD}	I_F = - 3 A, V_{GS} = 0 V		-	- 0.75	- 1.2	V

Notes

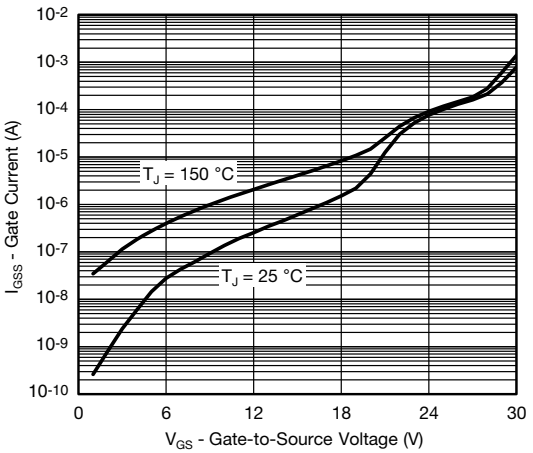
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

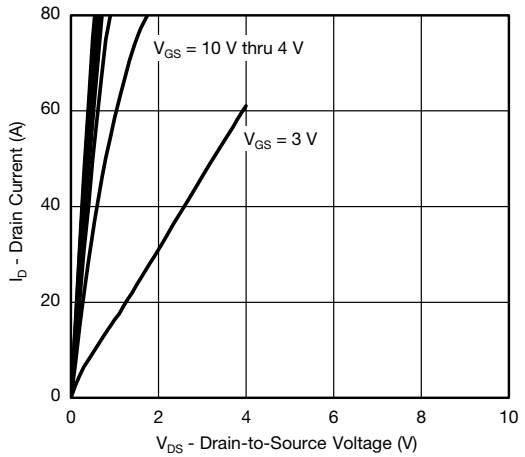
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



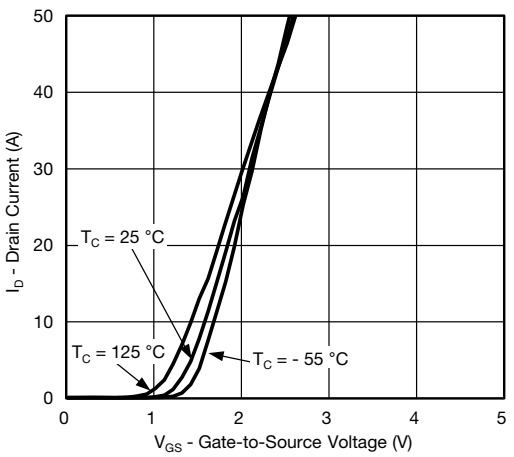
Gate Current vs. Gate-Source Voltage



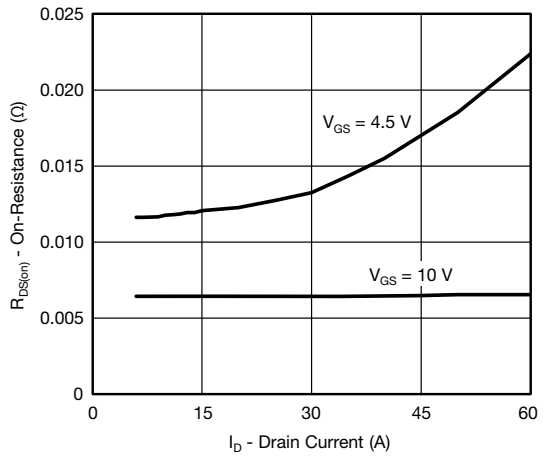
Gate Current vs. Gate-Source Voltage



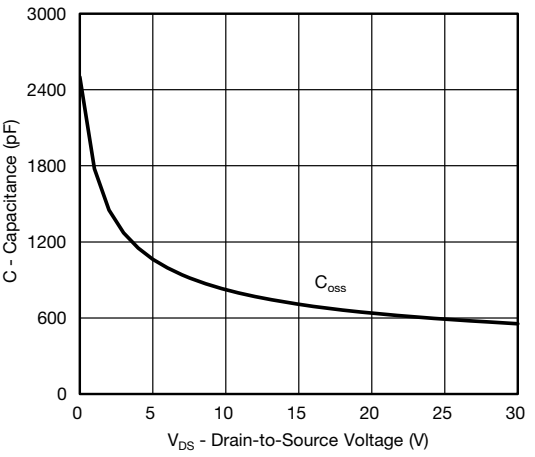
Output Characteristics



Transfer Characteristics

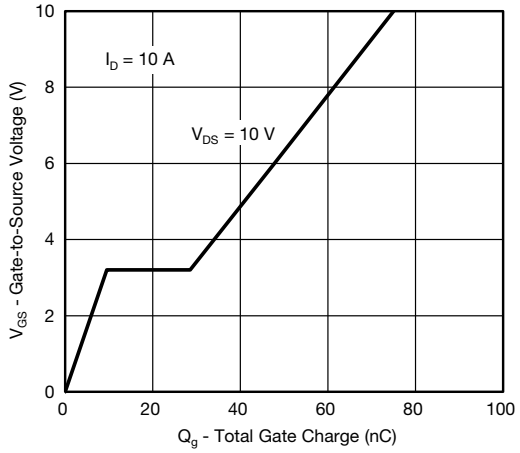


On-Resistance vs. Drain Current

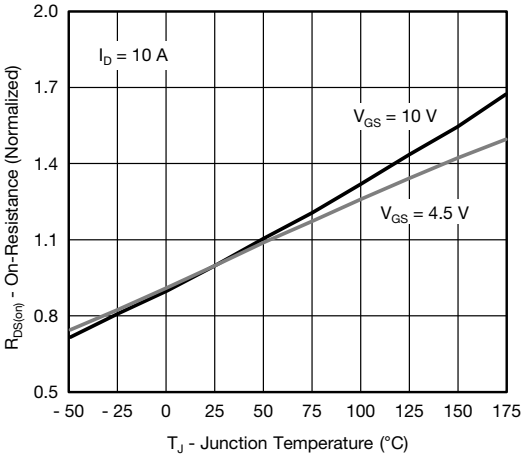


Capacitance

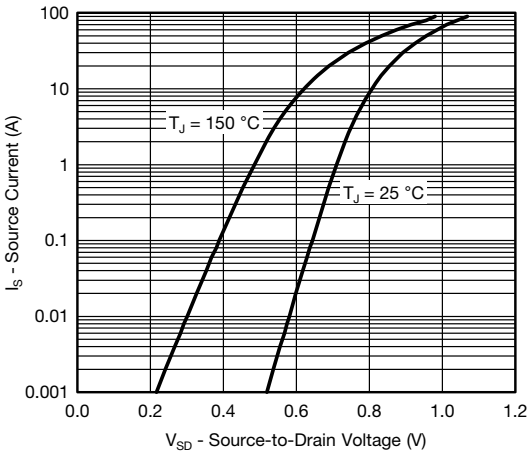
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



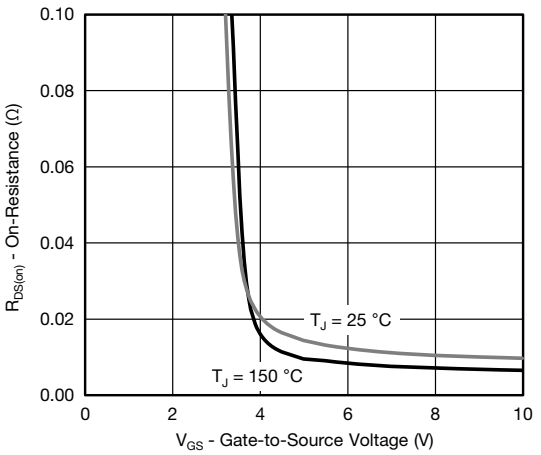
Gate Charge



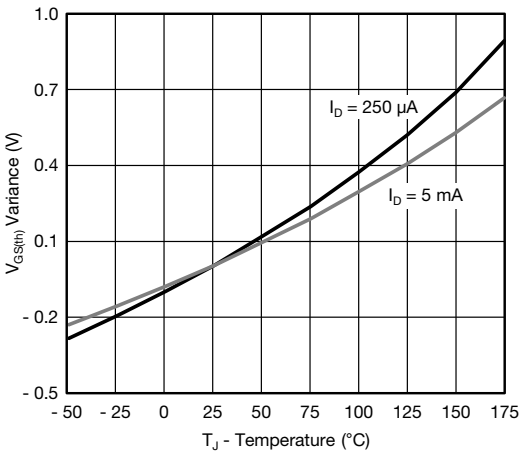
On-Resistance vs. Junction Temperature



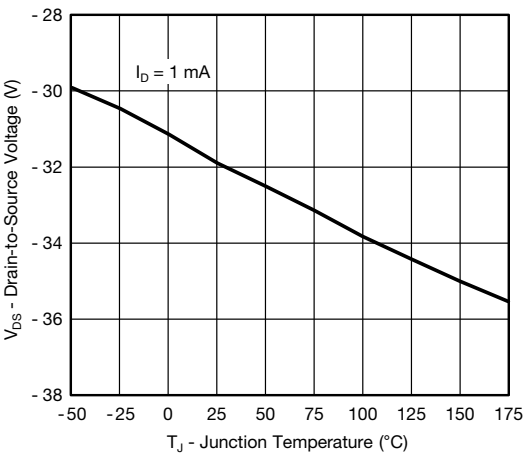
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

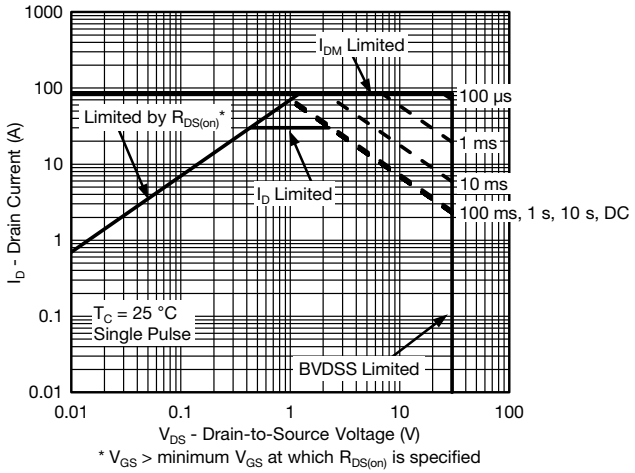


Threshold Voltage

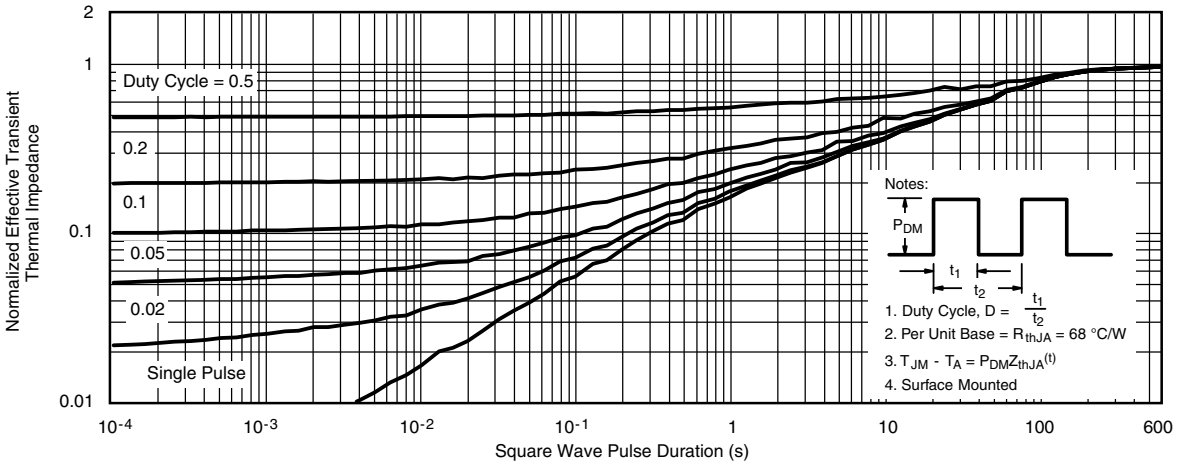


Drain Source Breakdown vs. Junction Temperature

THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)

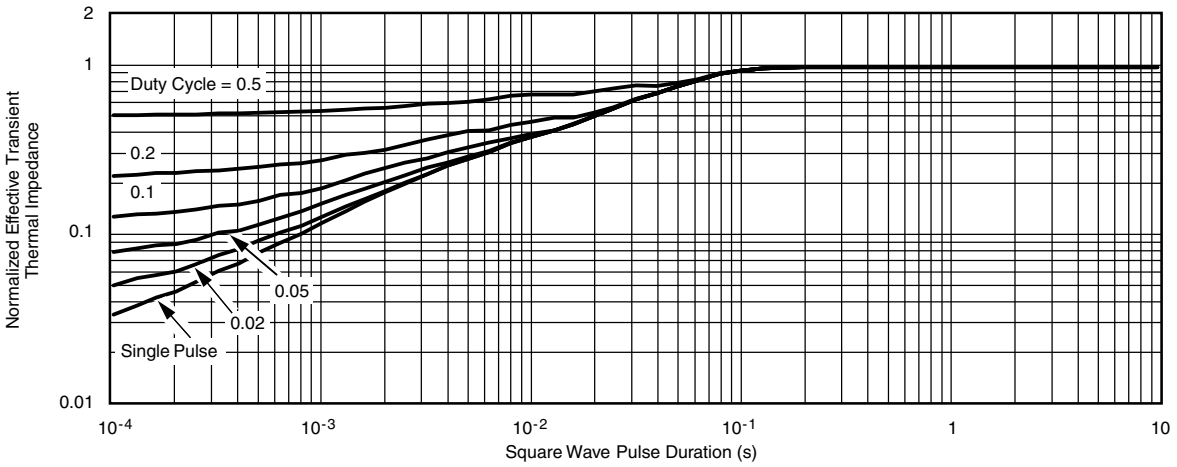


Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

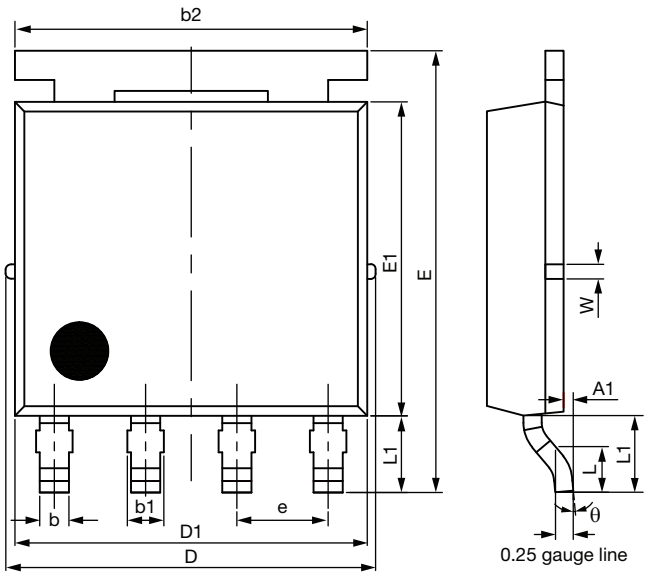
Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

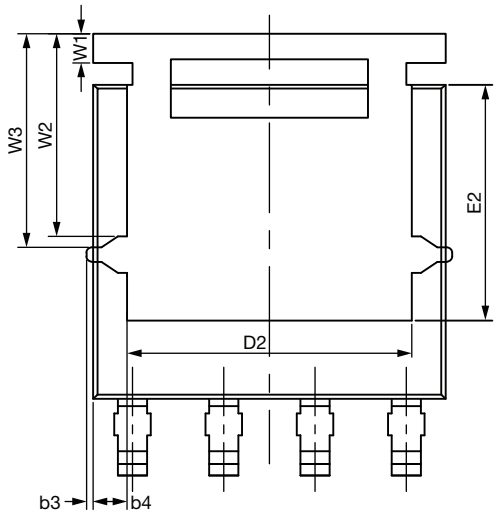
  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67076.

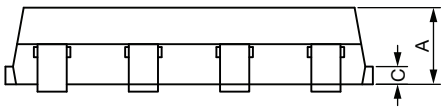
PowerPAK® SO-8L Case Outline for Non-Al Parts

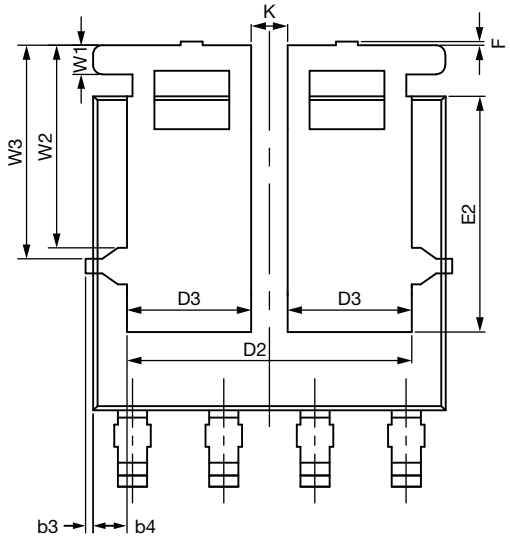


Topside view



Backside view (single)





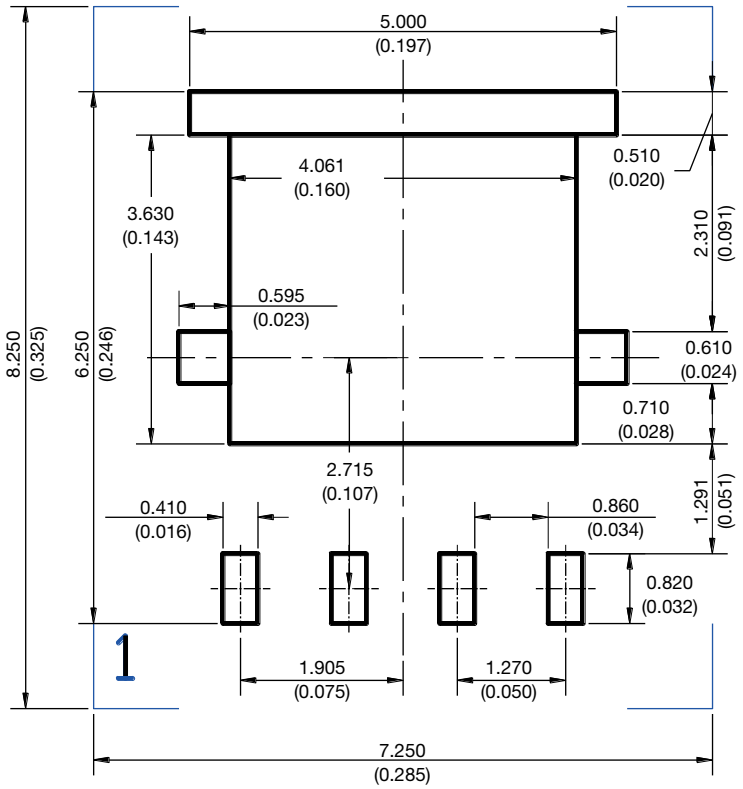
Backside view (dual)

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.094			0.004		
b4	0.47			0.019		
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	3.18	3.28	3.38	0.125	0.129	0.133
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.51			0.020		
W	0.23			0.009		
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		
θ	0°	-	10°	0°	-	10°
ECN: T16-0221-Rev. D, 16-May-16 DWG: 5976						

Note

- Millimeters will gover

RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads
Dimensions in mm (inches)

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