

Vishay Siliconix

N-Channel 20 V (D-S) MOSFET

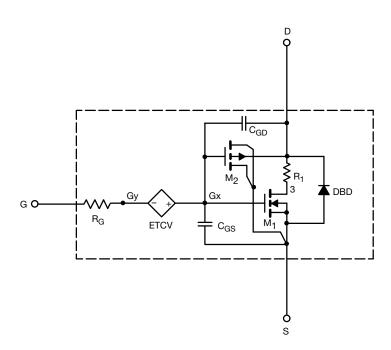
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- · Apply for both Linear and Switching Application
- Accurate over the 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



SPICE Device Model Si3464DV

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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.5	-	V
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 7.5 \text{ A}$	0.020	0.020	Ω
		V _{GS} = 2.5 V, I _D = 7 A	0.023	0.023	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 10 V, I _D = 7.5 A	20	17	S
Body Diode Voltage	V_{SD}	I _S = 6 A	0.77	0.75	V
Dynamic ^b					
Input Capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	1060	1065	pF
Output Capacitance	C _{oss}		126	150	
Reverse Transfer Capacitance	C _{rss}		60	70	
Total Gate Charge	Qg	$V_{DS} = 10 \text{ V}, V_{GS} = 5 \text{ V}, I_D = 7.5 \text{ A}$	10	12	nC
			9	11	
Gate-Source Charge	Q _{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 7.5 \text{ A}$	1.8	1.8	
Gate-Drain Charge	Q _{qd}	1	1.1	1.1	

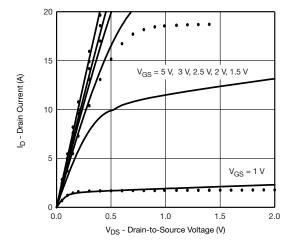
Notes

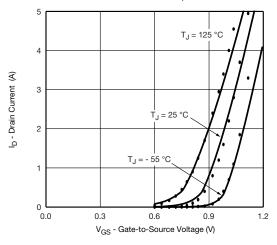
- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

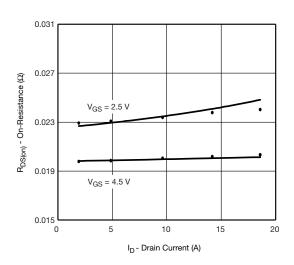
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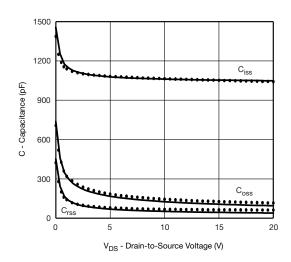
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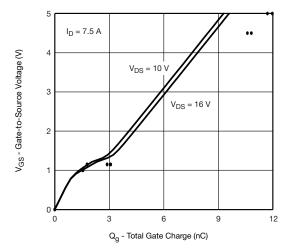
COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25$ °C, unless otherwise noted)

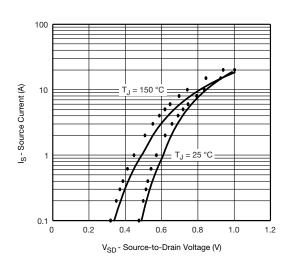












Note

• Dots and squares represent measured data.



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Revision: 02-Oct-12 Document Number: 91000