P-Channel 60 V (D-S) 175 °C MOSFET

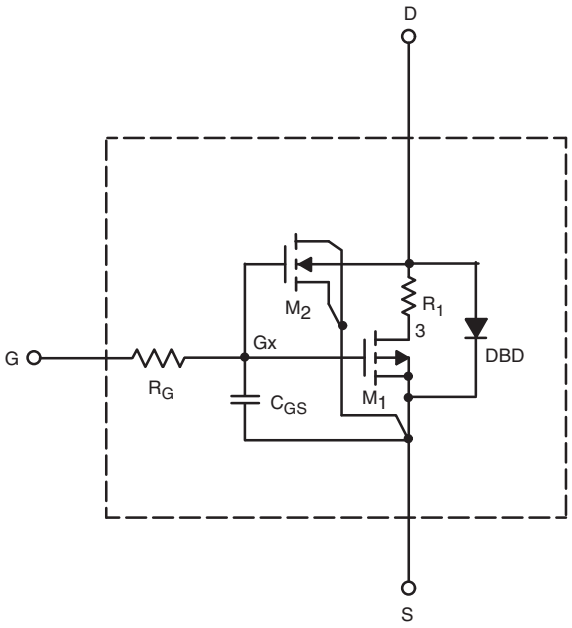
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

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SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)					
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static					
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	1.7	-	V
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 17 A	0.012	0.012	Ω
		V_{GS} = - 10 V, I_D = - 17 A, T_J = 125 °C	0.019	-	
		V_{GS} = - 10 V, I_D = - 17 A, T_J = 175 °C	0.023	-	
		V_{GS} = - 4.5 V, I_D = - 14 A	0.015	-	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 15 V, I_D = - 17 A	49	61	S
Diode Forward Voltage	V_{SD}	I_S = - 50 A, V_{GS} = 0 V	- 0.91	- 1	V
Dynamic[b]					
Input Capacitance	C_{iss}	V_{DS} = - 25 V, V_{GS} = 0 V, f = 1 MHz	5180	4950	pF
Output Capacitance	C_{oss}		497	480	
Reverse Transfer Capacitance	C_{rss}		455	405	
Total Gate Charge[c]	Q_g	V_{DS} = - 30 V, V_{GS} = - 10 V, I_D = - 50 A	100	110	nC
Gate-Source Charge[c]	Q_{gs}		19	19	
Gate-Drain Charge[c]	Q_{gd}		28	28	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = - 30 V, R_L = 0.60 Ω, $I_D \cong$ - 50 A, V_{GEN} = - 10 V, R_g = 2.5 Ω	31	15	ns
Rise Time[c]	t_r		29	70	
Turn-Off Delay Time[c]	$t_{d(off)}$		200	175	
Fall Time[c]	t_f		57	175	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = - 50 V, dI/dt = 100 A/µs	35	45	

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operting temperature.

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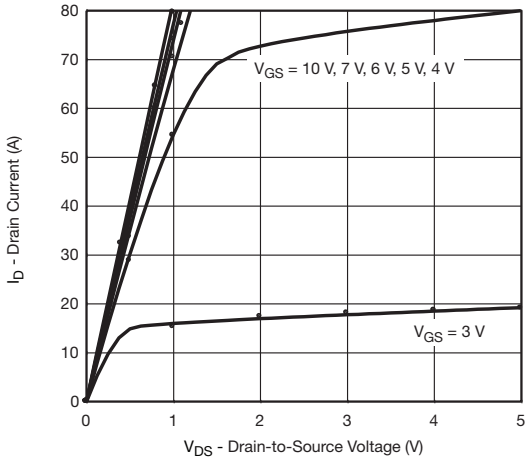
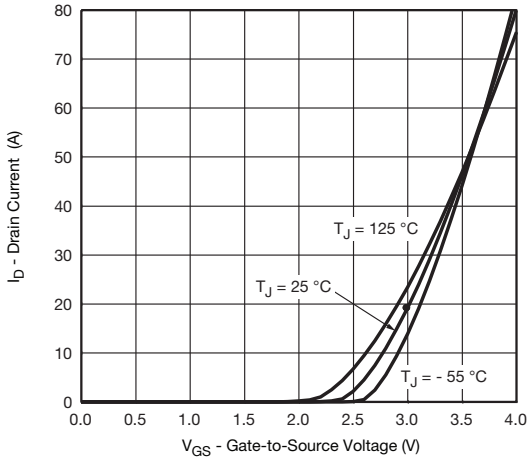
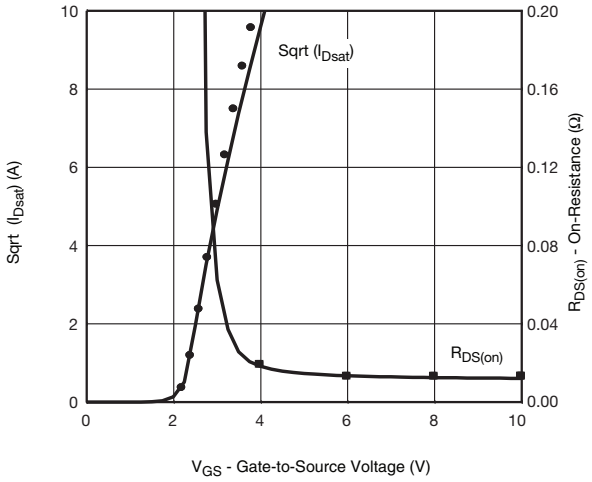
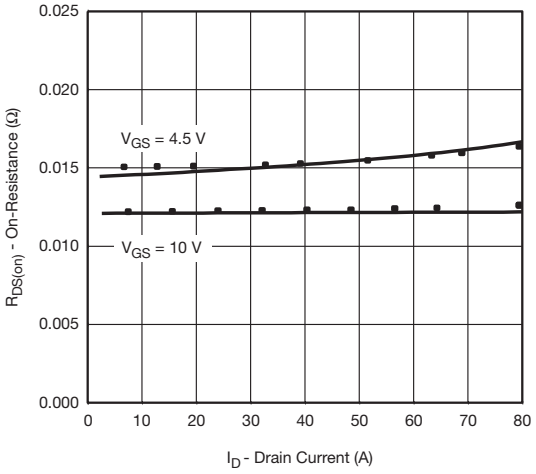
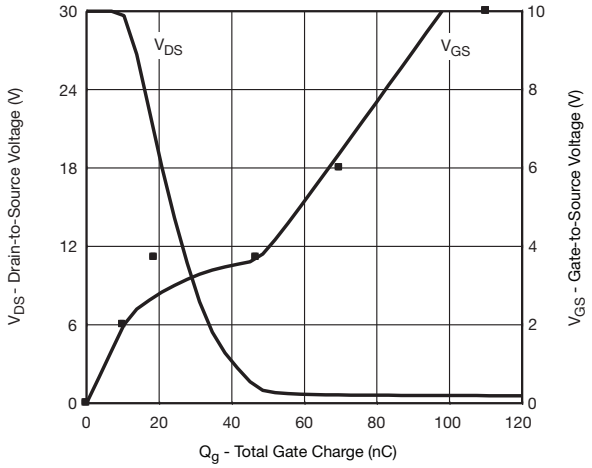
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)

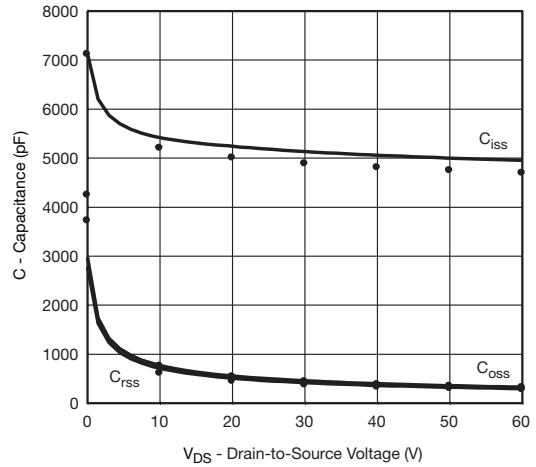












Note

- Dots and squares represent measured data.

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