

Vishay Siliconix

P-Channel 60 V (D-S) 175 °C MOSFET

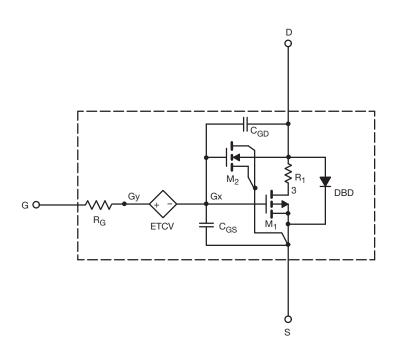
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - $55\,^{\circ}\text{C}$ to + $125\,^{\circ}\text{C}$ temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC



Note

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

SPICE Device Model SQ7415AEN

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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \mu A$	2.1	-	V
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = -10 \text{ V}, I_D = -5.7 \text{ A}$	0.044	0.050	Ω
		$V_{GS} = -4.5 \text{ V}, I_D = -4.4 \text{ A}$	0.074	0.070	
Forward Transconductancea	9 _{fs}	$V_{DS} = -15 \text{ V}, I_{D} = -5.7 \text{ A}$	8	13	S
Diode Forward Voltage	V_{SD}	I _S = - 6 A	- 0.85	- 0.85	V
Dynamic ^b					
Input Capacitance	C _{iss}	V _{DS} = - 25 V, V _{GS} = 0 V, f = 1 MHz	1110	1108	pF
Output Capacitance	Coss		131	132	
Reverse Transfer Capacitance	C _{rss}		81	84	
Total Gate Charge	Qg		22	25.5	
Gate-Source Charge	Q _{gs}	$V_{DS} = -30 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -5.7 \text{ A}$	3.6	3.6	nC
Gate-Drain Charge	Q _{gd}		6.7	6.7	

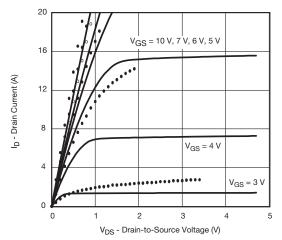
Notes

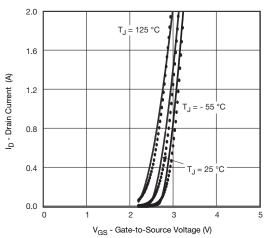
- a. Pulse test; pulse width $\leq 300~\mu s,\,duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

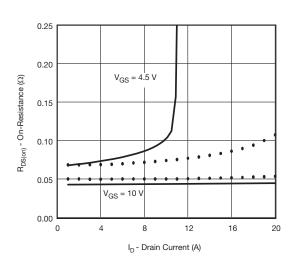


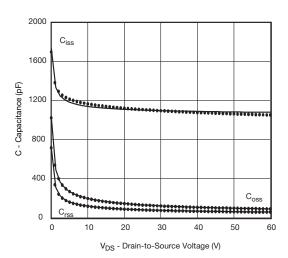
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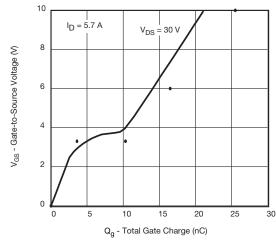
COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25$ °C, unless otherwise noted)

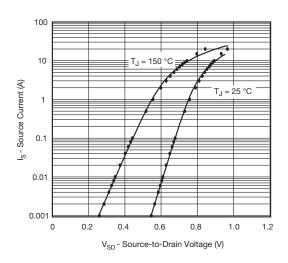












NoteDots and squares represent measured data.



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