# P-Channel 60 V (D-S) 175 °C MOSFET

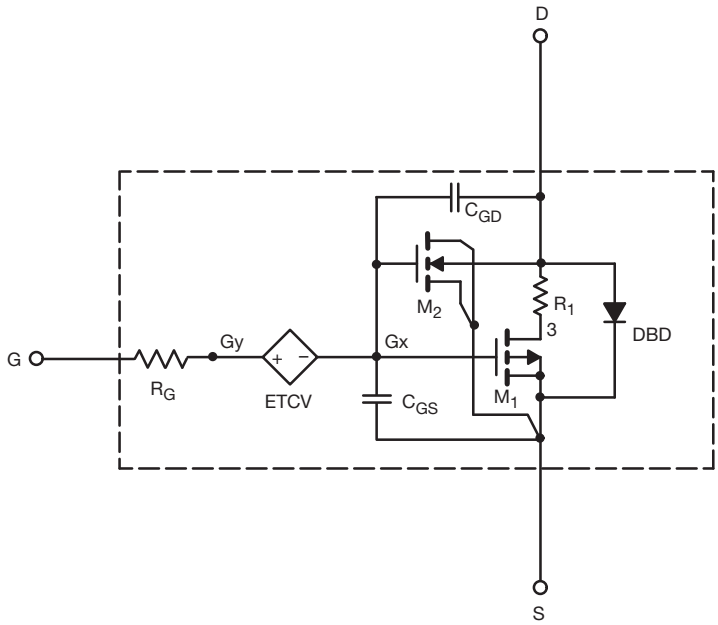
## DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

## CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

## SUBCIRCUIT MODEL SCHEMATIC




**Note**

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

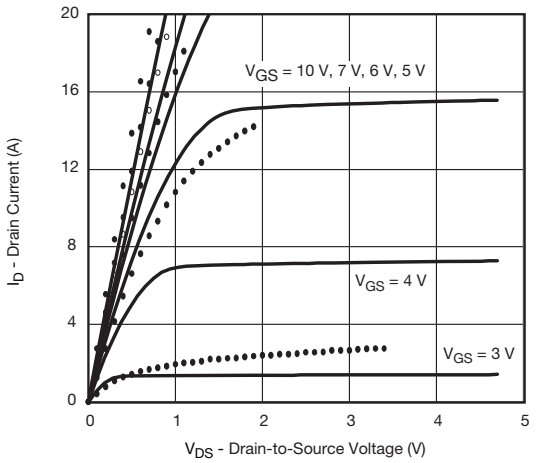
| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **SIMULATED DATA** | **MEASURED DATA** | **UNIT** |
| **Static** | | | | | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = - 250 µA | 2.1 | - | V |
| Drain-Source On-State Resistance[a] | $R_{DS(on)}$ | $V_{GS}$ = - 10 V, $I_D$ = - 5.7 A | 0.044 | 0.050 | Ω |
| | | $V_{GS}$ = - 4.5 V, $I_D$ = - 4.4 A | 0.074 | 0.070 | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = - 15 V, $I_D$ = - 5.7 A | 8 | 13 | S |
| Diode Forward Voltage | $V_{SD}$ | $I_S$ = - 6 A | - 0.85 | - 0.85 | V |
| **Dynamic[b]** | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = - 25 V, $V_{GS}$ = 0 V, f = 1 MHz | 1110 | 1108 | pF |
| Output Capacitance | $C_{oss}$ | | 131 | 132 | |
| Reverse Transfer Capacitance | $C_{rss}$ | | 81 | 84 | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = - 30 V, $V_{GS}$ = - 10 V, $I_D$ = - 5.7 A | 22 | 25.5 | nC |
| Gate-Source Charge | $Q_{gs}$ | | 3.6 | 3.6 | |
| Gate-Drain Charge | $Q_{gd}$ | | 6.7 | 6.7 | |

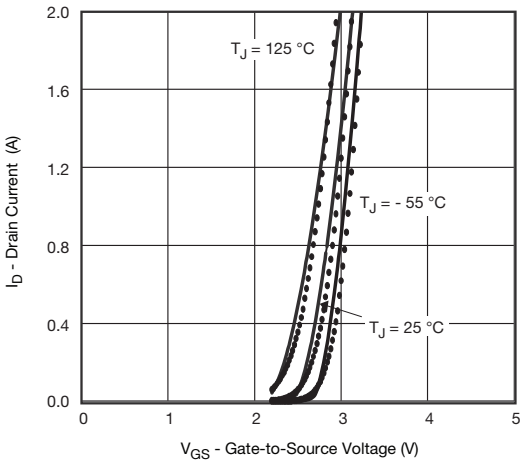
**Notes**

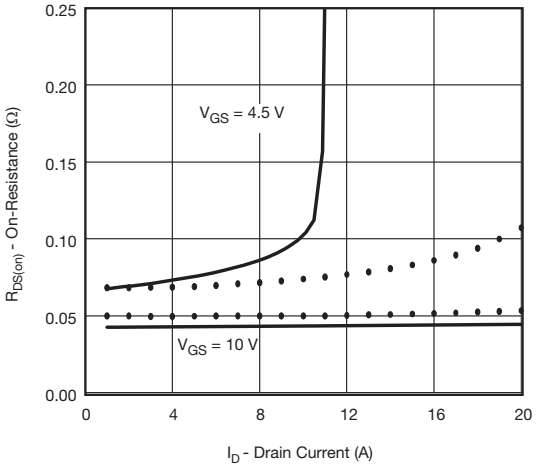
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

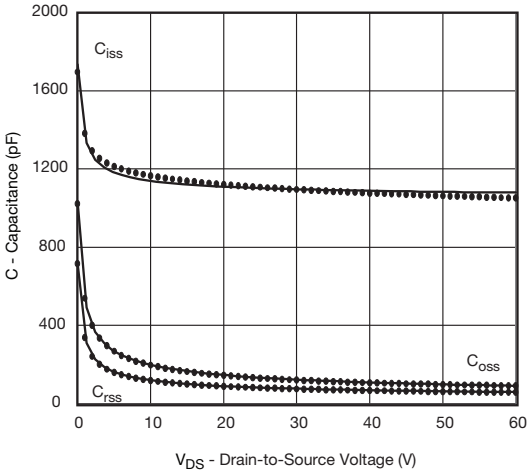
b. Guaranteed by design, not subject to production testing.

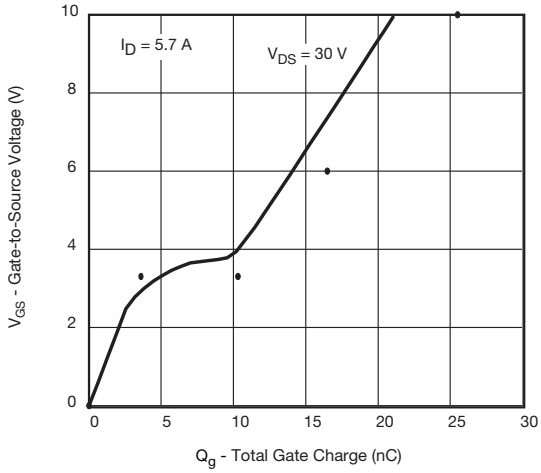
## COMPARISON OF MODEL WITH MEASURED DATA ($T_J$ = 25 °C, unless otherwise noted)

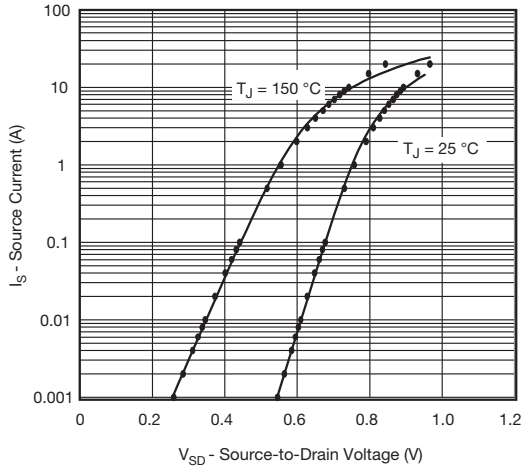



**Note**

Dots and squares represent measured data.