## **SQ9407EY**

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**Vishay Siliconix** 

## Automotive P-Channel 60 V (D-S) 175 °C MOSFET



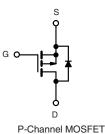
PRODUCT SUMMARY				
V <sub>DS</sub> (V)	-60			
$R_{DS(on)}(\Omega)$ at $V_{GS} = -10 \text{ V}$	0.085			
$R_{DS(on)}(\Omega)$ at $V_{GS} = -4.5 V$	0.115			
I <sub>D</sub> (A)	-4.6			
Configuration	Single			

#### **FEATURES**

- TrenchFET<sup>®</sup> power MOSFET
- AEC-Q101 qualified d
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



ROHS COMPLIANT HALOGEN FREE



ORDERING INFORMATION				
Package	SO-8			
Lead (Pb)-free and halogen-free	SQ9407EY (for detailed order number please see <u>www.vishay.com/doc?79771</u> )			

<b>ABSOLUTE MAXIMUM RATINGS</b> ( $T_C = 25 \degree C$ , unless otherwise noted)						
PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-source voltage		V <sub>DS</sub>	-60			
Gate-source voltage		V <sub>GS</sub>	± 20	V		
Continuous drain current	T <sub>C</sub> = 25 °C	1	-4.6			
Continuous drain current	T <sub>C</sub> = 125 °C	I <sub>D</sub>	-2.6			
Continuous source current (diode conduction)		I <sub>S</sub>	-3.4	А		
Pulsed drain current <sup>a</sup>		I <sub>DM</sub>	-18.5			
Single pulse avalanche current	L = 0.1 mH	I <sub>AS</sub>	-20			
Single pulse avalanche energy		E <sub>AS</sub>	20	mJ		
Maximum power dissipation <sup>a</sup>	T <sub>C</sub> = 25 °C	D	3.75	W		
	T <sub>C</sub> = 125 °C	P <sub>D</sub>	1.25	vv		
Operating junction and storage temperature rang	e	T <sub>J</sub> , T <sub>stg</sub>	-55 to + 175	°C		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-ambient	PCB mount <sup>b</sup>	R <sub>thJA</sub>	100	°C/W	
Junction-to-case (drain)		R <sub>thJF</sub>	40	0/10	

#### Notes

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %

b. When mounted on 1" square PCB (FR-4 material)

c. Parametric verification ongoing

S21-0849-Rev. B, 16-Aug-2021

1

Document Number: 67582

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PARAMETER	SYMBOL	vise noted) TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static	OTMEOL						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> =	= 0 V, I <sub>D</sub> = -250 μA	-60	-	-	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}, I_D = -250 \ \mu A$		-2.0	-2.5	V
Gate-source leakage	I <sub>GSS</sub>	-	$V_{DS} = 0 V, V_{GS} = \pm 20 V$		-	± 100	nA
Zero gate voltage drain current		V <sub>GS</sub> = 0 V	50 / 40		-	-1	ł – – –
	IDSS		V <sub>DS</sub> = -60 V, T <sub>J</sub> = 125 °C	-	-	-50	μA
		$V_{GS} = 0 V$	V <sub>DS</sub> = -60 V, T <sub>J</sub> = 175 °C	-	-	-150	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = -10 V	$V_{DS} \le -5 V$	-12	-	-	Α
		V <sub>GS</sub> = -4.5 V	I <sub>D</sub> = -2.5 A	-	0.087	0.115	
<b>5</b> · · · · · · ·		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -3.5 A	-	0.067	0.085	Ω
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V	I <sub>D</sub> = -3.5 A, T <sub>J</sub> = 125 °C	-	-	0.143	
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -3.5 A, T <sub>J</sub> = 175 °C	-	-	0.176	
Forward transconductance b	g <sub>fs</sub>	V <sub>DS</sub> =	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -3.5 A		10	-	S
Dynamic <sup>b</sup>					•		
Input capacitance	C <sub>iss</sub>		0 V V <sub>DS</sub> = -30 V, f = 1 MHz	-	912	1140	pF
Output capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$		-	100	125	
Reverse transfer capacitance	C <sub>rss</sub>			-	60	75	
Total gate charge <sup>c</sup>	Qg			-	26.5	40	
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = -10 V	$V_{DS} = -30 \text{ V}, \text{ I}_{D} = -4.3 \text{ A}$	-	3.8	-	nC
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	5.8	-	
Gate resistance	Rg		f = 1 MHz		7.1	10.7	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	$\begin{array}{l} V_{\text{DD}}=\text{-30 V, R}_{\text{L}}=8.8\ \Omega\\ I_{\text{D}}\cong\text{-3.4 A, V}_{\text{GEN}}=\text{-10 V, R}_{\text{g}}=1\ \Omega \end{array}$		-	11	17	
Rise time <sup>c</sup>	t <sub>r</sub>			-	13	20	- ns
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	36	54	
Fall time <sup>c</sup>	t <sub>f</sub>			-	8	12	
Source-Drain Diode Ratings and Cha	racteristics <sup>b</sup>						
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	-18.5	А
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = -3 A, V <sub>GS</sub> = 0 V		-	-0.84	-1.1	V

Notes

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %

b. Guaranteed by design, not subject to production testing

c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

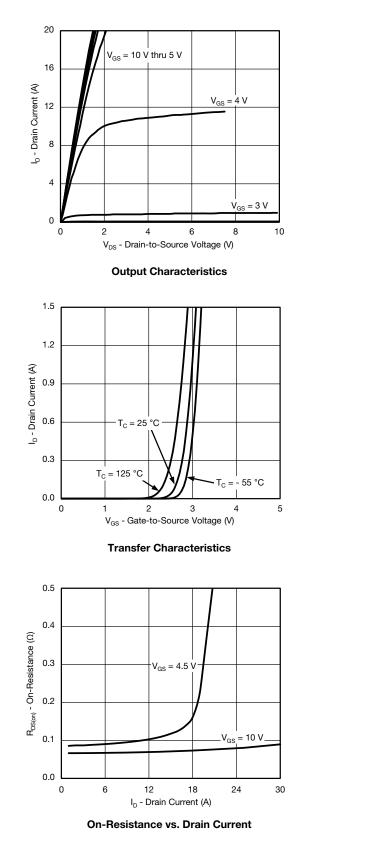
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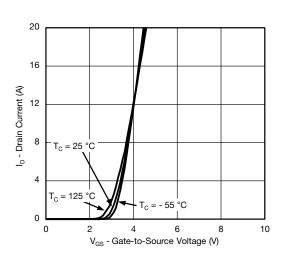


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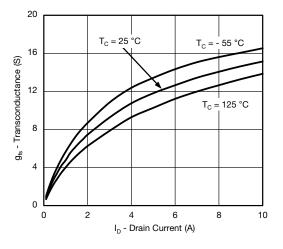
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#### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

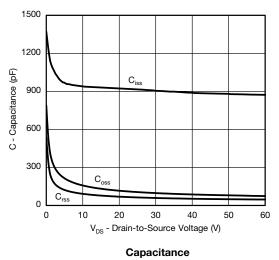




Transfer Characteristics







S21-0849-Rev. B, 16-Aug-2021

3

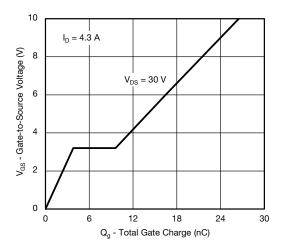
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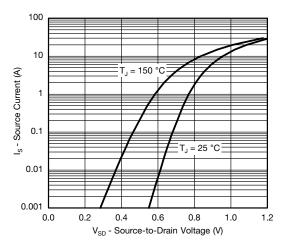


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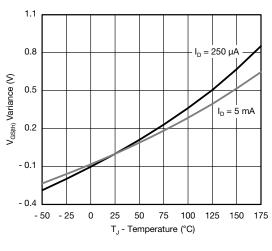
#### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



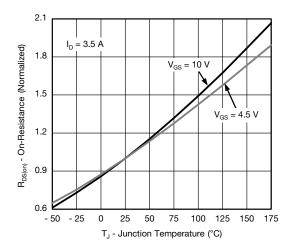
Gate Charge



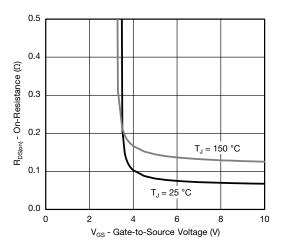
Source Drain Diode Forward Voltage



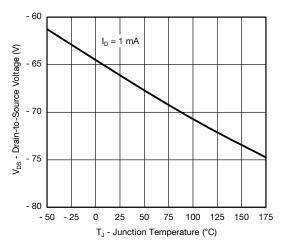
**Threshold Voltage** 



**On-Resistance vs. Junction Temperature** 



On-Resistance vs. Gate-to-Source Voltage



Drain Source Breakdown vs. Junction Temperature

S21-0849-Rev. B, 16-Aug-2021

4

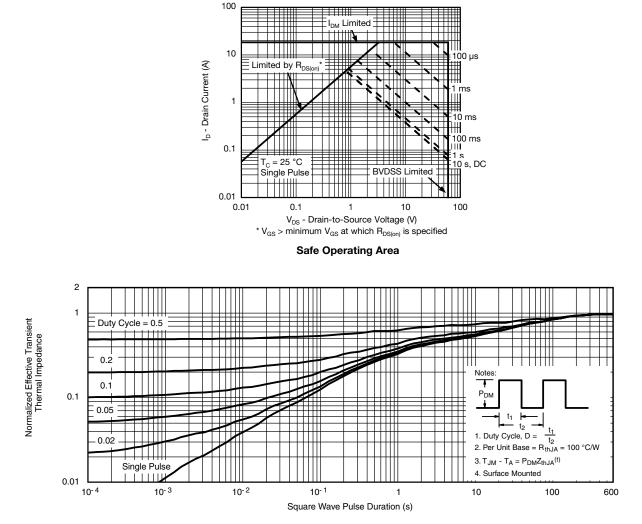
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#### **THERMAL RATINGS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)

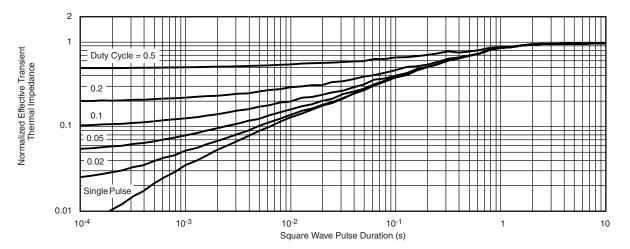


Normalized Thermal Transient Impedance, Junction-to-Ambient



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#### THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Foot

#### Note

The characteristics shown in the two graphs

- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

- Normalized Transient Thermal Impedance Junction-to-Foot (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67582.

6



## Package Information

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# SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012





	MILLIM	IETERS	INCHES		
DIM	Min	Мах	Min	Max	
A	1.35	1.75	0.053	0.069	
A <sub>1</sub>	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					

## **Application Note 826**

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**RECOMMENDED MINIMUM PADS FOR SO-8** 



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index



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Revision: 01-Jan-2025

1