SPICE Device Model SUP10250E



Vishay Siliconix

N-Channel 250 V (D-S) 175 °C MOSFET

DESCRIPTION

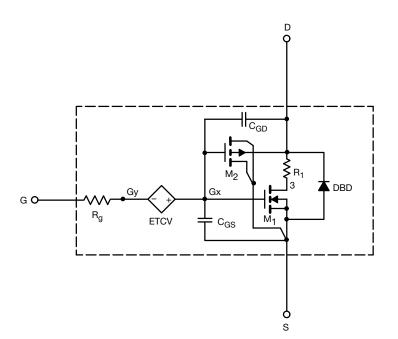
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched Cgd model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over -55 °C to +125 °C temperature range
- · Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



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| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | |
|--|---------------------|---|-------------------|------------------|------|
| PARAMETER | SYMBOL | TEST CONDITIONS | SIMULATED DATA | MEASURED DATA | UNIT |
| Static | | | | | |
| Gate-Source Threshold Voltage | V _{GS(th)} | $V_{DS}=V_{GS},\ I_{D}=250\ \mu A$ | 3 | - | V |
| Drain-Source On-State Resistance ^a | R _{DS(on)} | V_{GS} = 10 V, I _D = 30 A | 0.025 | 0.025 | Ω |
| | | V_{GS} = 7.5 V, I_D = 30 A | 0.026 | 0.026 | |
| Forward Transconductance ^a | g _{fs} | $V_{DS} = 15 \text{ V}, \text{ I}_{D} = 30 \text{ A}$ | 54 | 63 | S |
| Diode Forward Voltage | V _{SD} | I _S = 10 A | 0.78 | 0.79 | V |
| Dynamic ^b | | | | | |
| Input Capacitance | C _{iss} | V_{DS} = 125 V, V_{GS} = 0 V, f = 1 MHz | 3050 | 3002 | pF |
| Output Capacitance | Coss | | 171 | 184 | |
| Reverse Transfer Capacitance | C _{rss} | | 34 | 18 | |
| Total Gate Charge | Qg | V_{DS} = 125 V, V_{GS} = 10 V, I_{D} = 60 A | 56 | 57.6 | nC |
| Gate-Source Charge | Q _{gs} | | 15.1 | 15.1 | |
| Gate-Drain Charge | Q _{gd} | | 18.4 | 18.4 | |

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.



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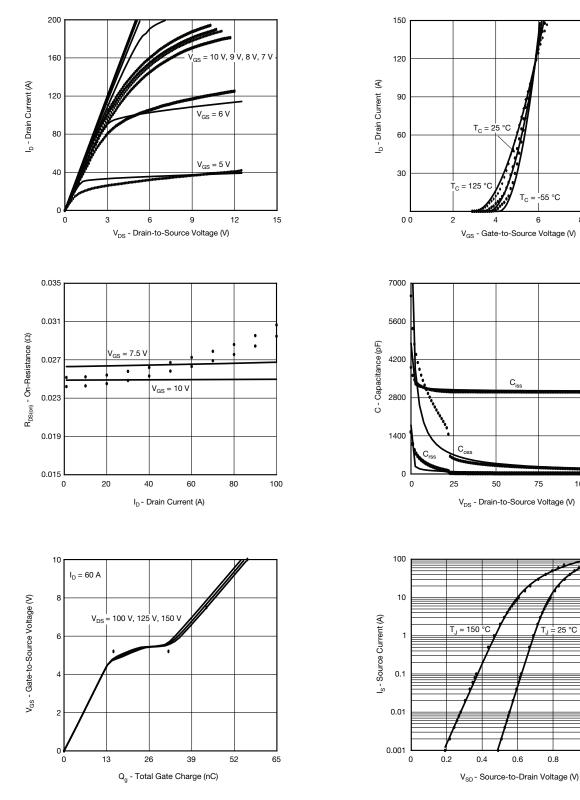
8

100

125

10

COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)



Note

• Dots and squares represent measured data. Copyright: Vishay Intertechnology, Inc.

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