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# Automotive N-Channel 80 V (D-S) 175 °C MOSFET

### DESCRIPTION

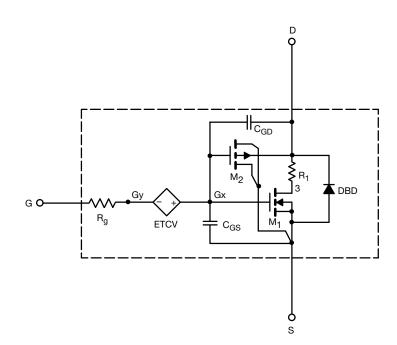
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

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A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- N-channel vertical DMOS
- · Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over -55 °C to +125 °C temperature range
- Model the gate charge



#### Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

## SUBCIRCUIT MODEL SCHEMATIC





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<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS}=V_{GS},\ I_{D}=250\ \mu A$	3	3	V
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	0.0180	0.0179	Ω
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 10 \text{ A}$	24	24	S
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 10 A	0.85	0.86	V
Dynamic <sup>b</sup>					
Input Capacitance	C <sub>iss</sub>	$V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1 MHz	910	875	pF
Output Capacitance	C <sub>oss</sub>		470	460	
Reverse Transfer Capacitance	C <sub>rss</sub>		41	25	
Total Gate Charge	Qg		13.4	14	
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 40 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 2.5 \text{ A}$	4	4	nC
Gate-Drain Charge	Q <sub>gd</sub>		3	3	

Notes

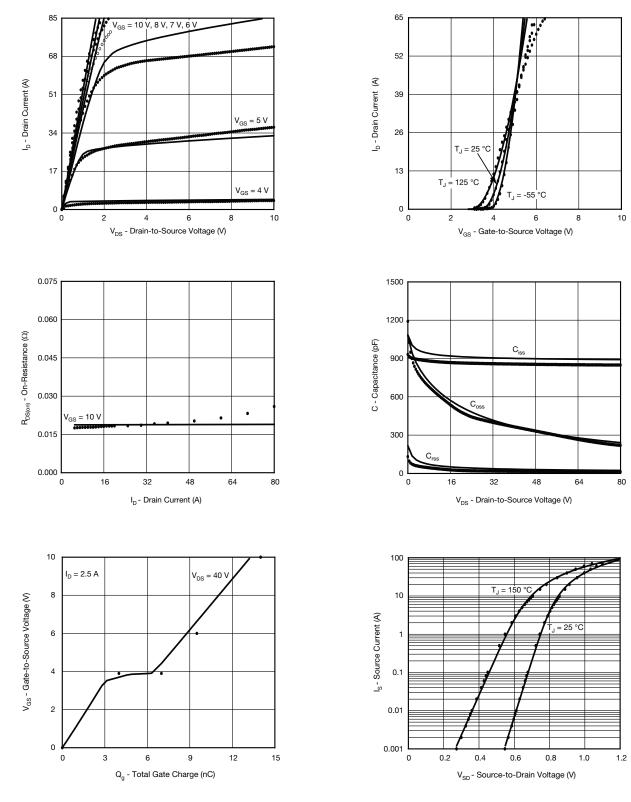
a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.



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# COMPARISON OF MODEL WITH MEASURED DATA (T<sub>J</sub> = 25 °C, unless otherwise noted)



#### Note

• Dots and squares represent measured data. Copyright: Vishay Intertechnology, Inc.

S17-1375-Rev. A, 04-Sep-17

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Document Number: 67762

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