2 Port, USB 2.0 High Speed (480 Mbps) Switch, DPDT Analog Switch

DESCRIPTION

The DG2730 is 2 port high speed analog switch optimized for USB 2.0 signal switching. The DG2730 switch is configured in DPDT. It handles bidirectional signal flow, achieving a 900 MHz -3 dB bandwidth, a port to port crosstalk at -36 dB and isolation at -29 dB, measured at 240 MHz.

Processed with high density sub micron CMOS, the DG2730 provide low parasitic capacitance. Signals are routed with minimized phase distortion and attain a bit to bit skew is as low as 40 ps.

The DG2730 is designed for a wide range of operating voltages, from 2.7 V to 5.5 V that can be driven directly from one cell Li-ion battery or 5 V power supply. On-chip circuitry protects against conditions when either the D+ / D- lines are shorted to the V_{BUS} at the USB port. Additionally, logic control pins (S and $\overline{OE}$) can tolerate the presence of voltages that are above the supply power rail (V+). The control logic threshold is guaranteed to be (V_{IH} = 1.3 V/min up to V+ = 3.6 V). Latch up current is 500 mA, as per JESD78, and its ESD tolerance exceeds 5.5 kV.

Packaged in ultra small miniQFN-10 (1.4 mm x 1.8 mm x 0.55 mm), it is ideal for portable high speed mix signal switching application.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device termination. The miniQFN-10 package has a nickel-palladium-gold device termination and is represented by the lead (Pb)-free "-GE4" suffix to the ordering part number. The nickel-palladium-gold device terminations meet all JEDEC® standards for reflow and MSL rating.

As a further sign of Vishay Siliconix's commitment, the DG2730 is fully RoHS-complaint.

FEATURES

- Wide operation voltage range
- Low on-resistance, 5.5 Ω (typical at 3 V)
- Low capacitance, C_{ON} = 5.8 pF (typical)
- 3 dB high bandwidth: 900 MHz (typical)
- Low bit to bit skew: 40 ps (typical)
- Low power consumption
- Low logic threshold: V
- Power down protection: D+, D-, HSD1+, HSD1-, HSD2+, and HSD2- pins can tolerate up to 5.5 V when V+ = 0 V
- 5.5 kV ESD protection (HBM)
- Latch-up current 500 mA per JESD78
- Lead (Pb)-free low profile miniQFN-10 (1.4 mm x 1.8 mm x 0.55 mm)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

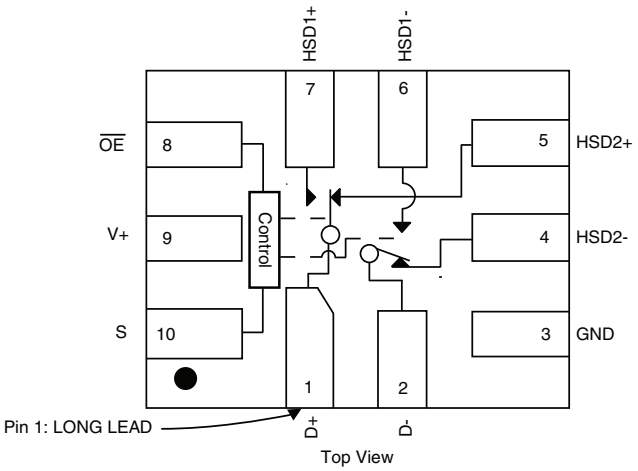
Pb-free
RoHS COMPLIANT
HALOGEN FREE

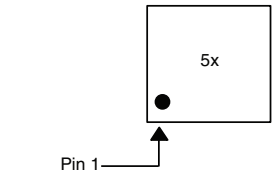
APPLICATIONS

- Cellular phones
- Portable media players
- PDA
- Digital camera
- GPS
- Notebook computer
- TV, monitor, and set top box

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

miniQFN-10L





Device marking: 5x for DG2730
x = Date/Lot Traceability Code

ORDERING INFROMATION		
TEMP. RANGE	**PACKAGE**	**PART NUMBER**
-40 °C to +85 °C	miniQFN-10	DG2730DN-T1-GE4

TRUTH TABLE		
$\overline{OE}$ (PIN 8)	**S (PIN 10)**	**FUNCTION**
0	1	D+ = HSD1+ and D- = HSD1-
0	0	D+ = HSD2+ and D- = HSD2-
1	X	Disconnect

PIN DESCRIPTIONS	
PIN NAME	**DESCRIPTION**
$\overline{OE}$	Bus switch enable
S	Select input
HSD1±, HSD2±, D±	Data port

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)			
PARAMETER		**LIMIT**	**UNIT**
Reference to GND	V+, D±, HSD1±, HSD2±	-0.3 to +6	V
	S, $\overline{OE}$ [a]	-0.3 to (V+ + 0.3)	
Current (Any terminal except S, $\overline{OE}$, D±, HSD1±, HSD2±)		30	mA
Continuous current (S, $\overline{OE}$, D±, HSD1±, HSD2±)		± 250	
Peak current (pulsed at 1 ms, 10 % duty cycle)		± 500	
Storage temperature (D suffix)		-65 to +150	°C
Power dissipation (packages) [b]	miniQFN-10 [c]	208	mW
ESD (human body model)		5.5	kV
Latch-up (current injection)		500	mA

Notes

a. Signals on S, $\overline{OE}$, exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings
b. All leads welded or soldered to PC board
c. Derate 2.6 mW/°C above 70 °C

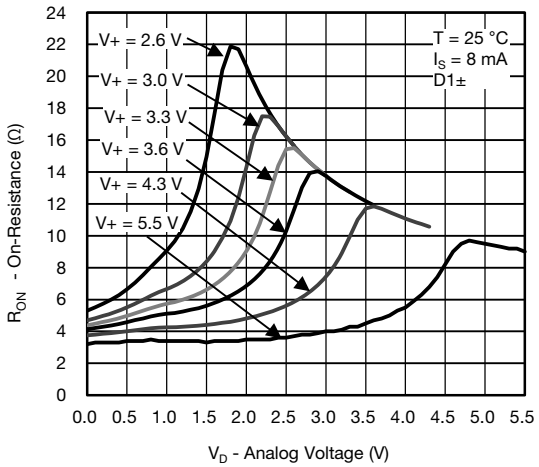
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V+ = 3 V)							
PARAMETER	SYMBOL	TEST CONDITIONS OTHERWISE UNLESS SPECIFIED	TEMP. [a]	LIMITS -40 °C to +85 °C			UNIT
				MIN. [b]	TYP. [c]	MAX. [b]	
Analog Switch							
Analog signal range [d]	V_{ANALOG}	$R_{DS(on)}$	Full	0	-	V+	V
On-resistance	$R_{DS(on)}$	V+ = 3 V, $I_{D±}$ = 8 mA, $V_{HSD1/2±}$ = 0.4 V	Room	-	5.5	8	Ω
			Full	-	-	9	
On-resistance match [d]	ΔR_{ON}	V+ = 3 V, $I_{D±}$ = 8 mA, $V_{HSD1/2±}$ = 0.4 V	Room	-	0.8	-	
On-resistance flatness [d]	R_{ON} Flatness	V+ = 3 V, $I_{D±}$ = 8 mA, $V_{HSD1/2±}$ = 0 V, 1 V	Room	-	2	-	
Switch off leakage current	I_{off}	V+ = 4.3 V, $V_{HSD1/2±}$ = 0.3 V, 3 V, $V_{D±}$ = 3 V, 0.3 V	Full	-100	-	100	nA
Channel on leakage current	I_{on}	V+ = 4.3 V, $V_{HSD1/2±}$ = 0.3 V, 4 V, $V_{D±}$ = 4 V, 0.3 V	Full	-200	-	200	
Digital Control							
Input voltage high	V_{INH}	V+ = 3 V to 3.6 V	Full	1.3	-	-	V
		V+ = 4.3 V	Full	1.5	-	-	
Input voltage low	V_{INL}	V+ = 3 V to 4.3 V	Full	-	-	0.5	
Input capacitance	C_{IN}		Full	-	6.5	-	pF
Input current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	-1	-	1	µA
Dynamic Characteristics							
Break-before-make time [d]	t_{BBM}	V+ = 3 V, $V_{D1/2\ ±}$ = 1.5 V, R_L = 50 Ω, C_L = 35 pF	Room	-	5	-	ns
			Full	-	5	-	
S, $\overline{OE}$ turn-on time [d]	t_{ON}		Room	-	-	30	
			Full	-	-	30	
S, $\overline{OE}$ turn-off time [d]	t_{OFF}		Room	-	-	25	
			Full	-	-	25	
Charge injection [d]	Q_{INJ}	C_L = 1 nF, R_{GEN} = 0 Ω, V_{GEN} = 0 V	Room	-	3	-	pC
Off-isolation [d]	OIRR	V+ = 3 V to 3.6 V, R_L = 50 Ω, C_L = 5 pF, f = 240 MHz		-	-29	-	dB
Crosstalk [d, e]	X_{TALK}			-	-36	-	
Bandwidth [d]	BW	V+ = 3 V to 3.6 V, R_L = 50 Ω, - 3 dB		-	900	-	MHz
D+/D- on capacitance	C_{ON}	V+ = 3.3 V, $\overline{OE}$ = 0 V, f = 240 MHz		-	5.8	-	pF
D1n, D2n off capacitance	C_{OFF}	V+ = $\overline{OE}$ = 3.3 V, f = 240 MHz		-	2.2	-	
Channel-to-channel skew [d]	$t_{SK(O)}$	V+ = 3 V to 3.6 V, R_L = 50 Ω, C_L = 5 pF		-	50	-	ps
Skew off opposite transitions of the same output [d]	$t_{SK(p)}$			-	20	-	
Total jitter [d]	t_J			-	200	-	
Power Supply							
Power supply range	V+		-	2.6	-	5.5	V
Power supply current	I+	V_{IN} = 0 V, or V+	Full	-	-	2	µA

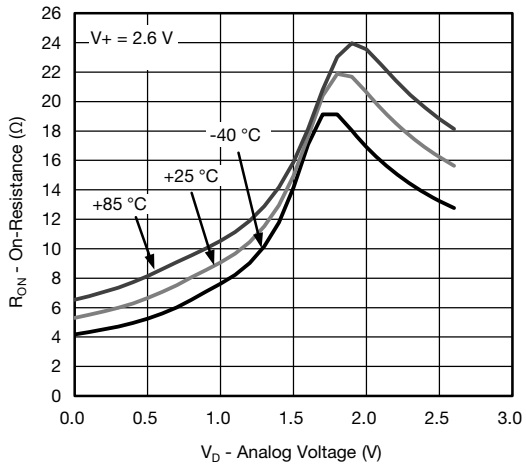
Notes

a. Room = 25 °C, Full = as determined by the operating suffix
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
c. Typical values are for design aid only, not guaranteed nor subject to production testing
d. Guaranteed by design, not subjected to production test
e. Crosstalk measured between channels

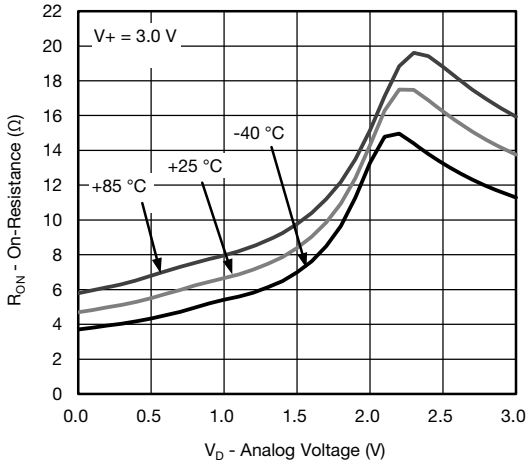
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



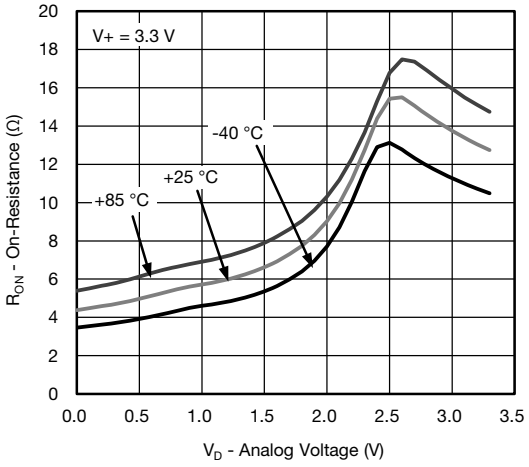
R_{ON} vs. V_D and Single Supply Voltage



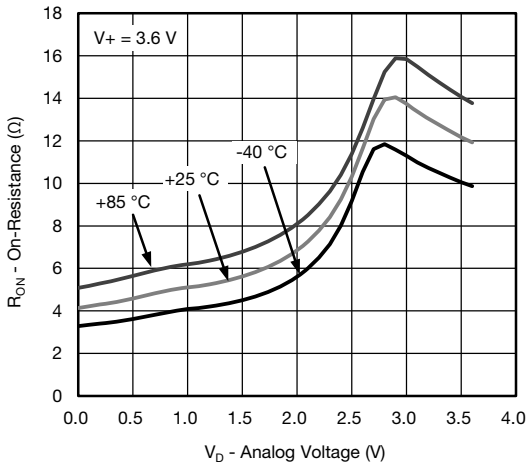
R_{ON} vs. Analog Voltage and Temperature



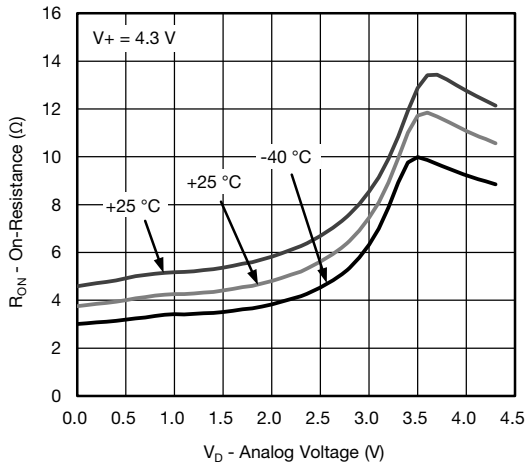
R_{ON} vs. Analog Voltage and Temperature



R_{ON} vs. Analog Voltage and Temperature

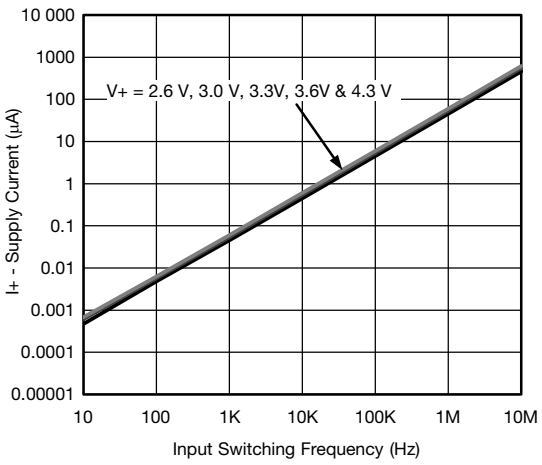


R_{ON} vs. Analog Voltage and Temperature

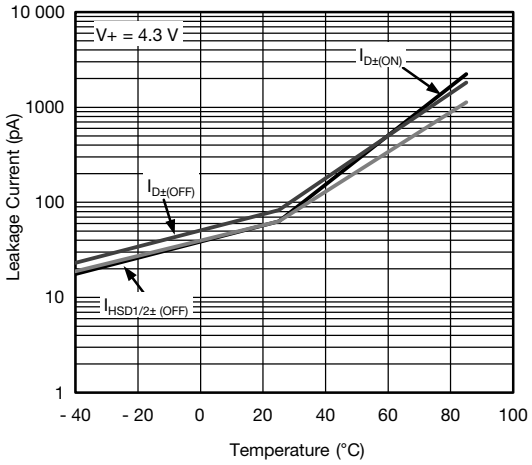


R_{ON} vs. Analog Voltage and Temperature

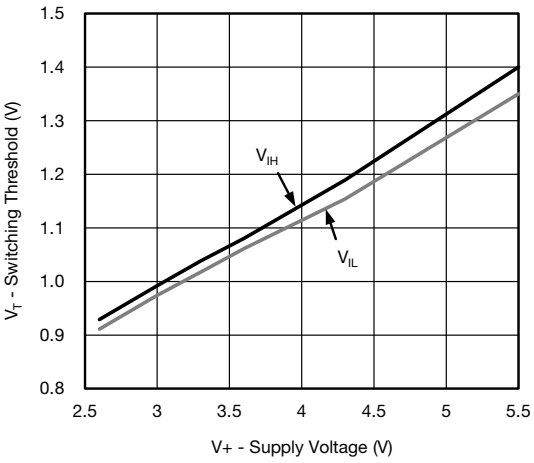
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



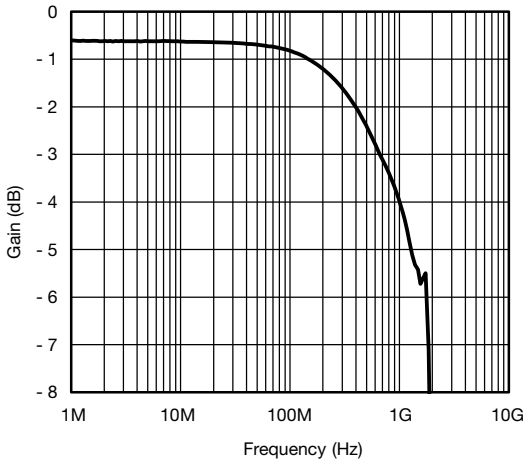
Supply Current vs. Input Switching Frequency



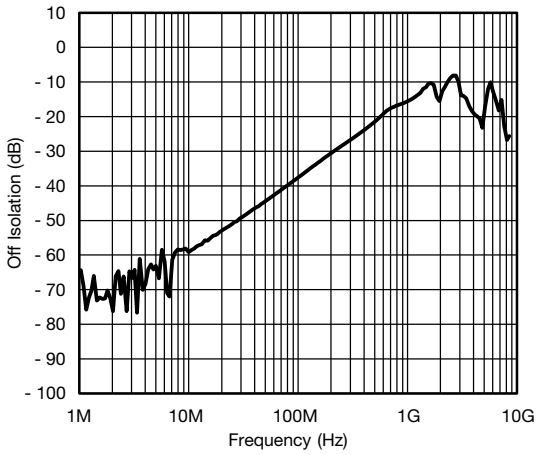
Leakage Current vs. Temperature



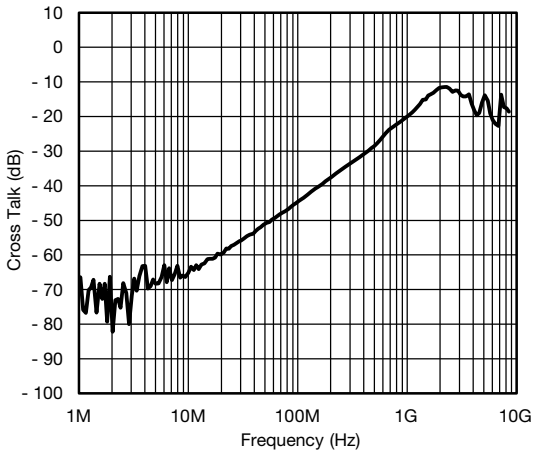
Switching Threshold vs. Supply Voltage



Gain vs. Frequency, V+ = 3.3 V

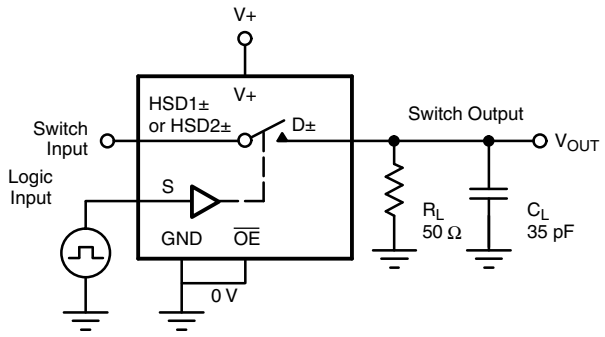


Off-Isolation, V+ = 3.3 V



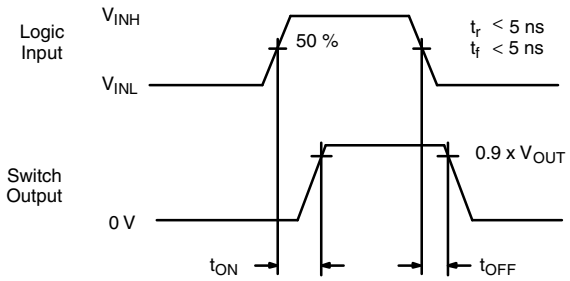
Crosstalk, V+ = 3.3 V

TEST CIRCUITS



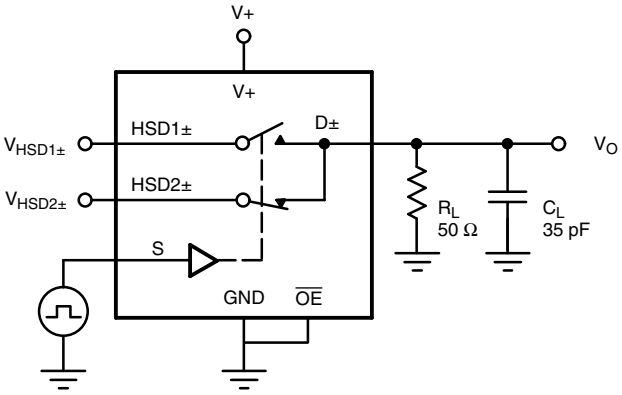
C_L (includes fixture and stray capacitance)

$$V_{OUT} = D\pm \left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch on
Logic input waveforms inverted for switches that have the opposite logic sense.

Fig. 1 - Switching Time



C_L (includes fixture and stray capacitance)

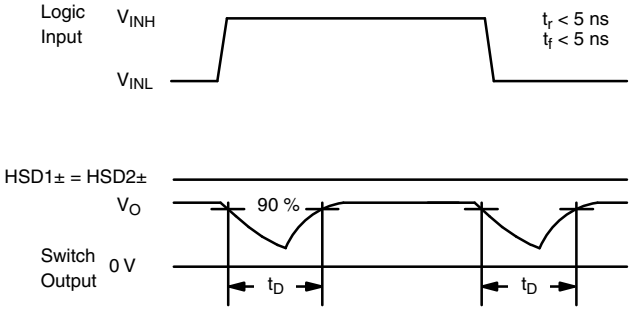
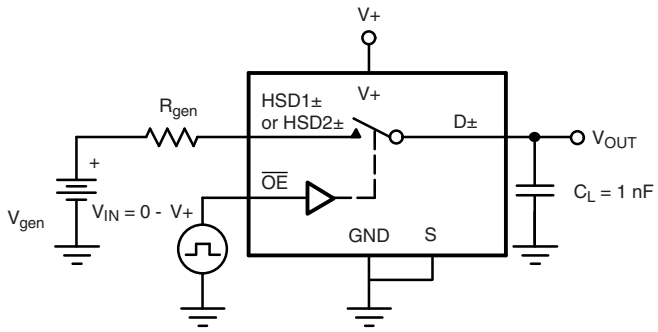
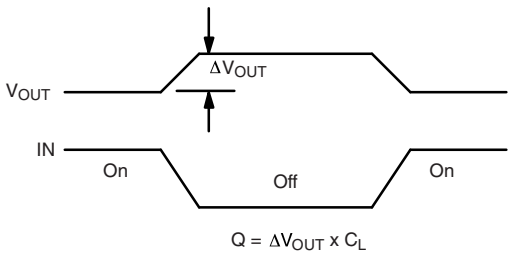


Fig. 2 - Break-Before-Make Interval





Q = ΔV$_{OUT}$ x C_L

IN depends on switch configuration: input polarity determined by sense of switch.

Fig. 3 - Charge Injection

TEST CIRCUITS

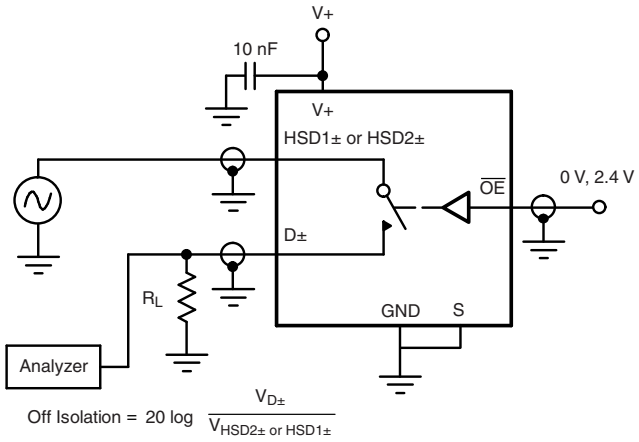


Fig. 4 - Off-Isolation

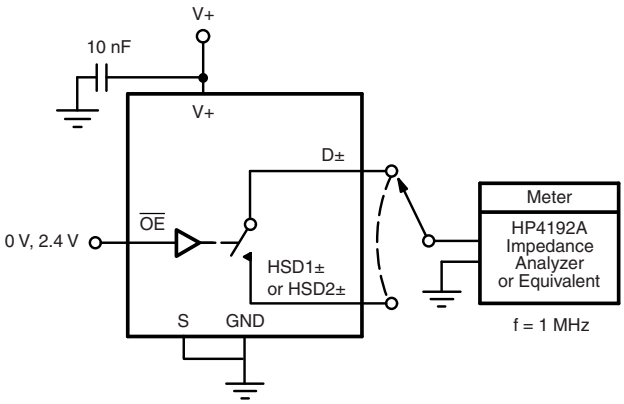


Fig. 5 - Channel Off/On Capacitance

PRODUCT SUMMARY	
Part number	DG2730
Status code	2
Configuration	DPDT x 1
Single supply min. (V)	2.7
Single supply max. (V)	5.5
Dual supply min. (V)	-
Dual supply max. (V)	-
On-resistance (Ω)	5.5
Charge injection (pC)	3
Source on capacitance (pF)	5.8
Source off capacitance (pF)	2.2
Leakage switch on typ. (nA)	-
Leakage switch off max. (nA)	100
-3 dB bandwidth (MHz)	900
Package	miniQFN-10
Functional circuit / applications	Multi purpose, USB, portable
Interface	Binary
Single supply operation	Yes
Dual supply operation	-
Turn on time max. (ns)	30
Crosstalk and off isolation	-36

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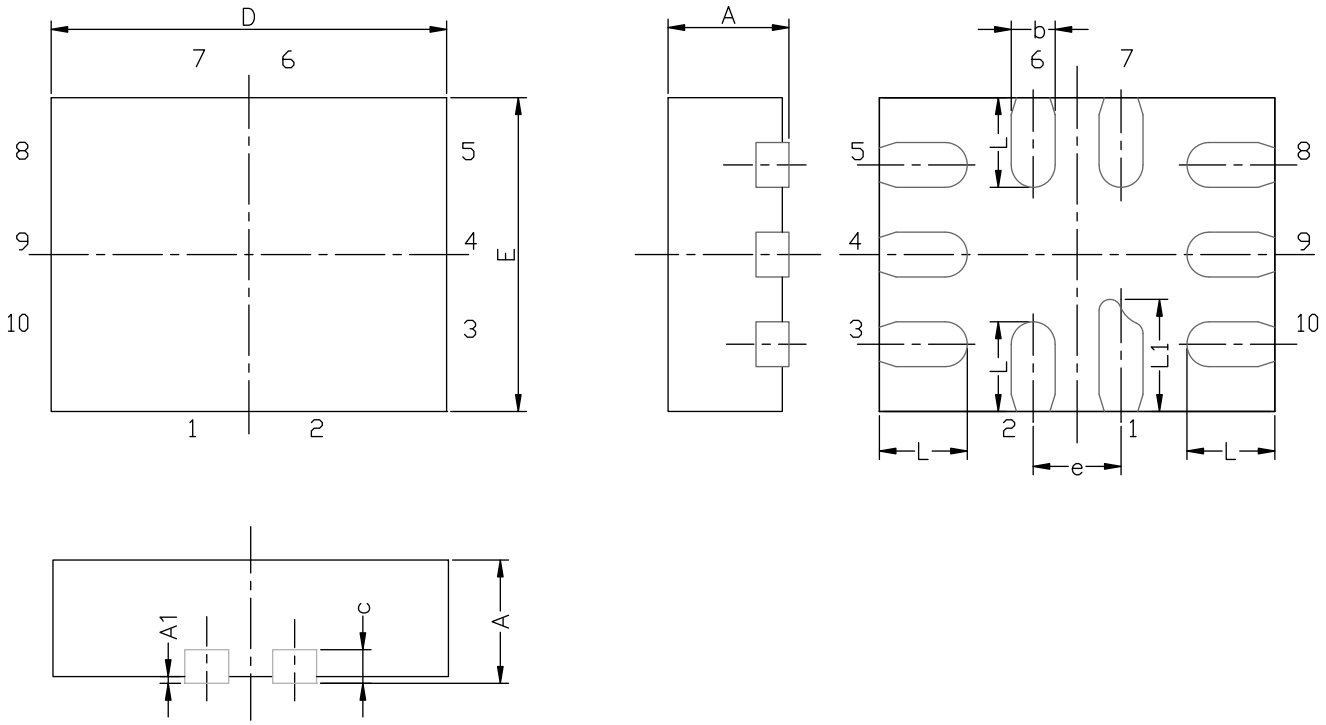
MINI QFN-10L CASE OUTLINE



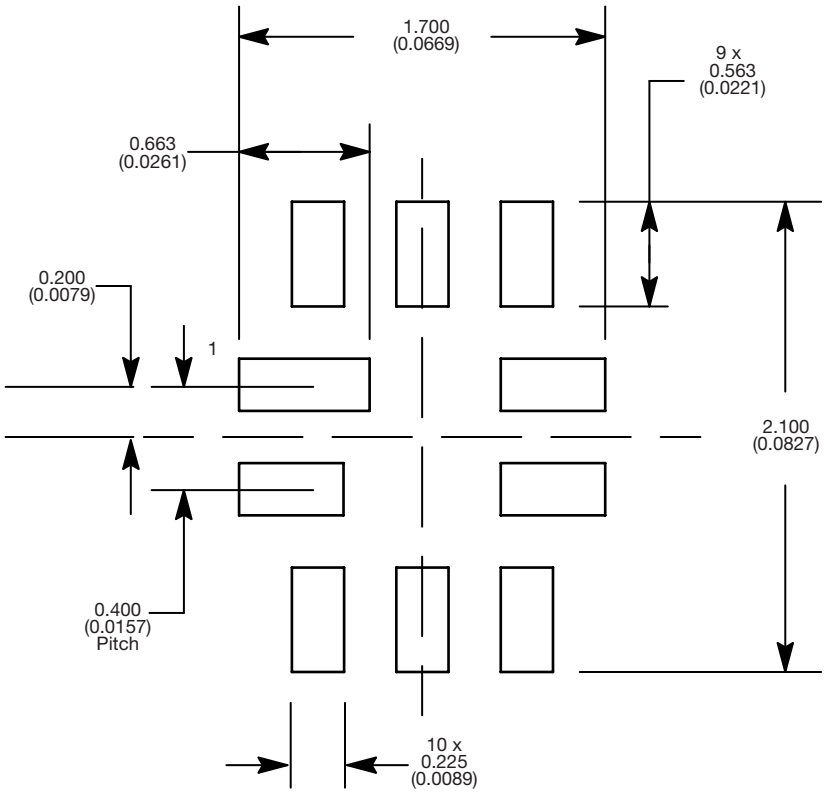
DIM	MILLIMETERS			INCHES		
	MIN.	NAM.	MAX.	MIN.	NAM.	MAX.
A	0.45	0.55	0.60	0.0177	0.0217	0.0236
A1	0.00	-	0.05	0.000	-	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.150 or 0.127 REF (1)			0.006 or 0.005 REF (1)		
D	1.70	1.80	1.90	0.067	0.071	0.075
E	1.30	1.40	1.50	0.051	0.055	0.059
e	0.40 BSC			0.016 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.45	0.50	0.55	0.0177	0.0197	0.0217

Note

(1) The dimension depends on the leadframe that assembly house used.

ECN T16-0163-Rev. B, 16-May-16
DWG: 5957

RECOMMENDED MINIMUM PADS FOR MINI QFN 10L



Mounting Footprint
Dimensions in mm (inch)

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