

N-Channel and P-Channel 40 V (D-S) 175 °C MOSFET

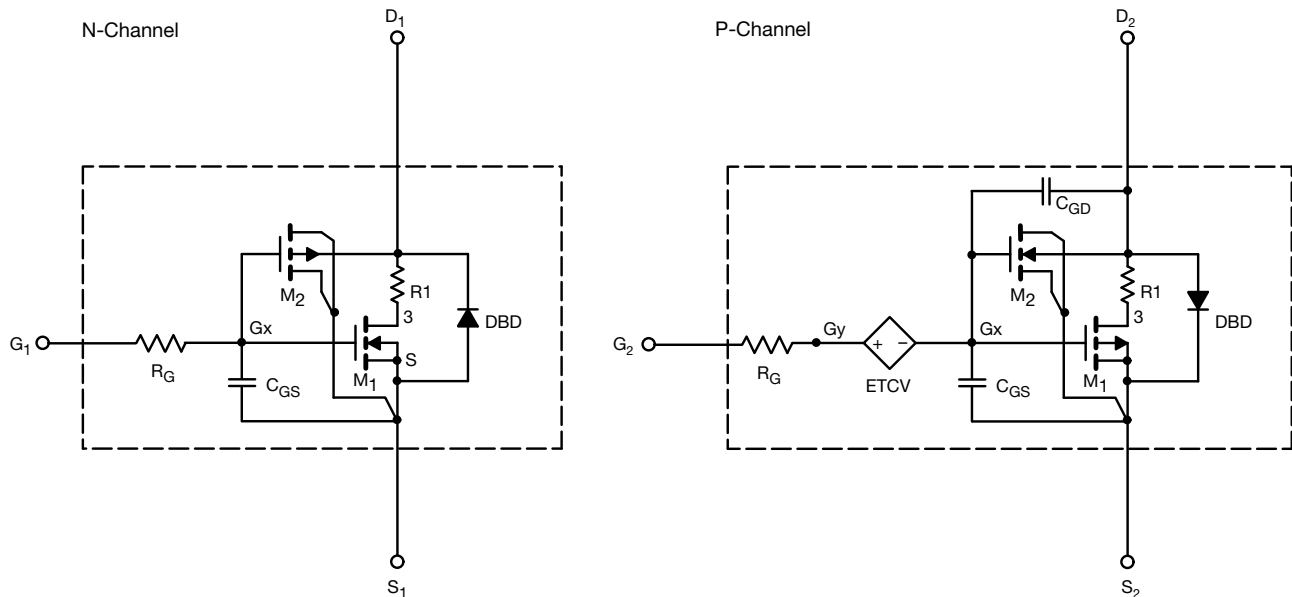
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the N-channel and P-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

CHARACTERISTICS

- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

SPICE Device Model SQJ500EP

Vishay Siliconix



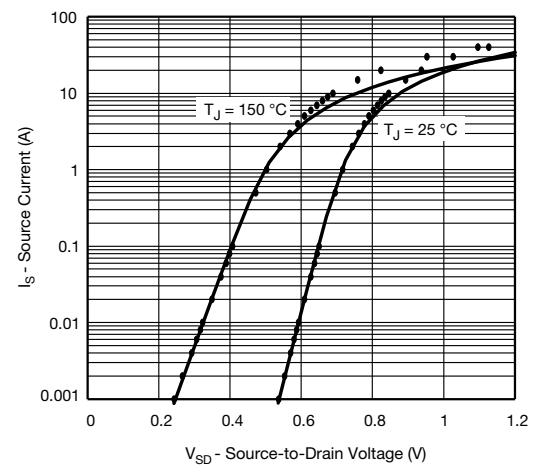
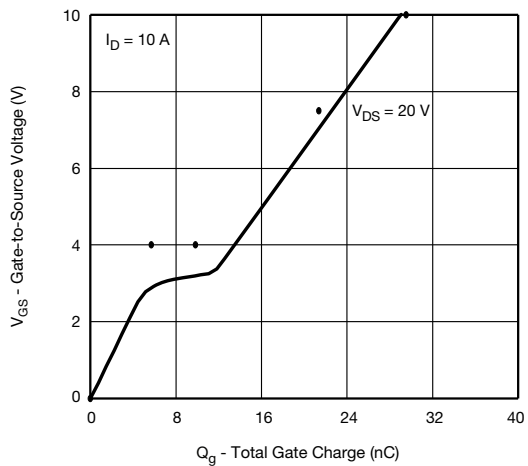
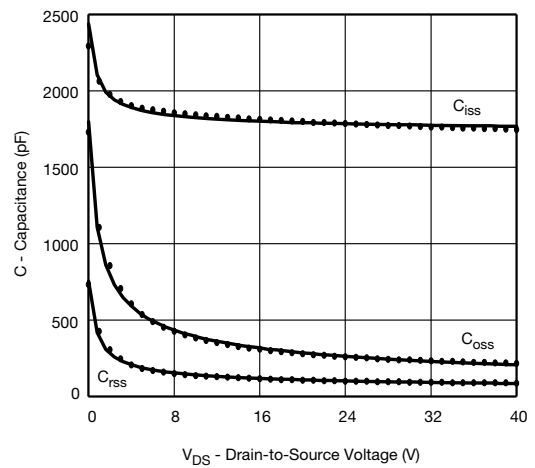
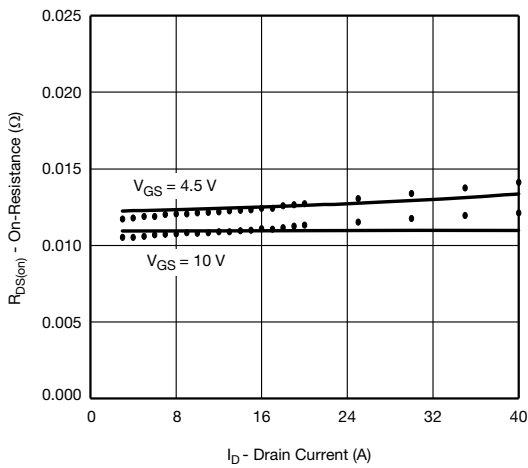
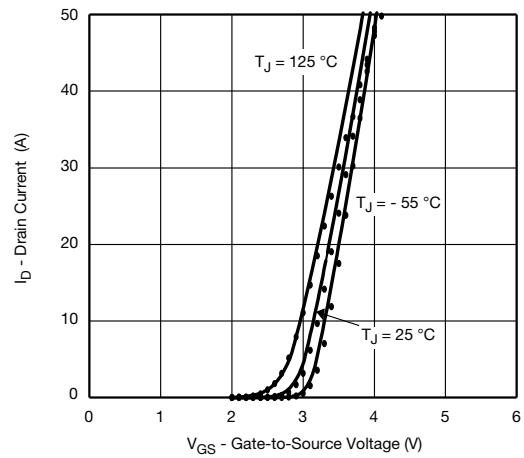
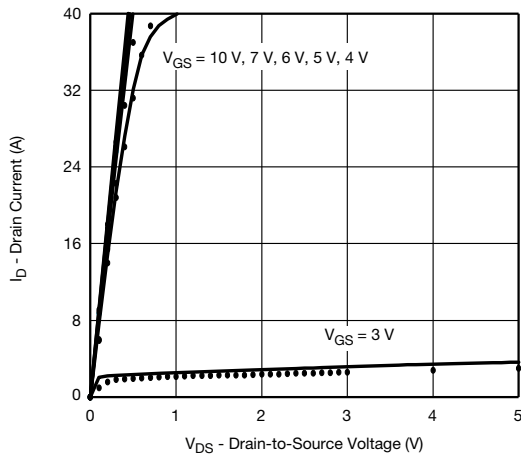
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS		SIMULATED DATA	MEASURED DATA	UNIT
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	1.9	-	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	1.8	-	
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 8\text{ A}$	N-Ch	0.011	0.011	Ω
		$V_{GS} = -10\text{ V}, I_D = -8\text{ A}$	P-Ch	0.022	0.022	
		$V_{GS} = 4.5\text{ V}, I_D = 6\text{ A}$	N-Ch	0.012	0.012	
		$V_{GS} = -4.5\text{ V}, I_D = -6\text{ A}$	P-Ch	0.034	0.033	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 8\text{ A}$	N-Ch	39	40	S
		$V_{DS} = -15\text{ V}, I_D = -8\text{ A}$	P-Ch	17	18	
Diode Forward Voltage ^a	V_{SD}	$I_S = 4\text{ A}, V_{GS} = 0\text{ V}$	N-Ch	0.78	0.79	V
		$I_S = -4\text{ A}, V_{GS} = 0\text{ V}$	P-Ch	0.81	0.82	
Dynamic^b						
Input Capacitance	C_{iss}	N-Channel $V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch	1790	1799	pF
			P-Ch	1790	1756	
Output Capacitance	C_{oss}	P-Channel $V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch	287	282	
			P-Ch	305	296	
Reverse Transfer Capacitance	C_{rss}		N-Ch	110	109	
			P-Ch	191	208	
Total Gate Charge	Q_g	N-Channel $V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	N-Ch	30	31.5	nC
			P-Ch	36	41.5	
Gate-Source Charge	Q_{gs}	P-Channel $V_{DS} = -20\text{ V}, V_{GS} = -10\text{ V}, I_D = -10\text{ A}$	N-Ch	5.7	5.7	
			P-Ch	5.5	5.5	
Gate-Drain Charge	Q_{gd}		N-Ch	4.8	4.8	
			P-Ch	10.5	10.5	

Notes

- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)

N-Channel MOSFET

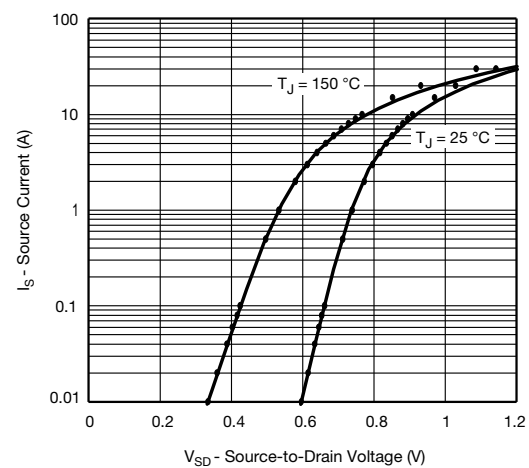
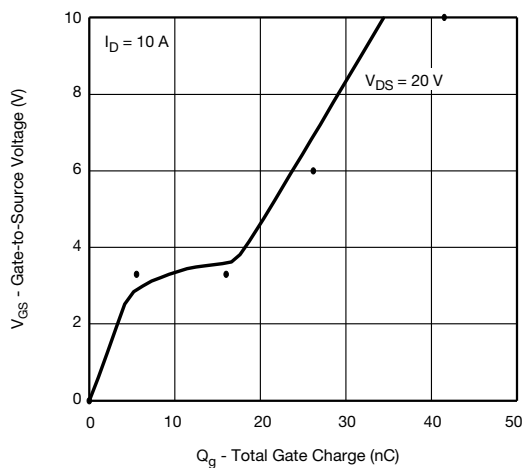
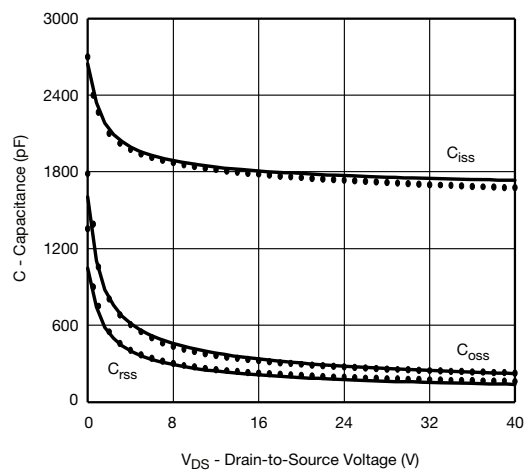
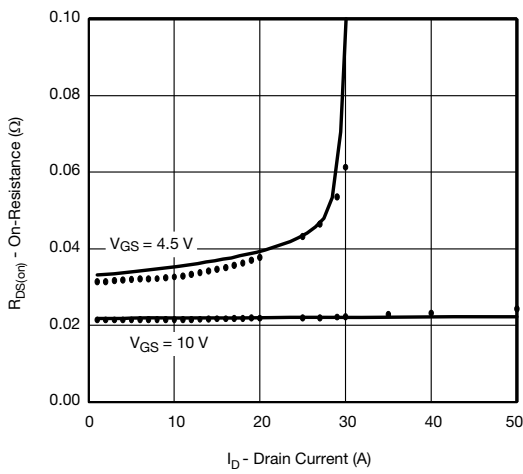
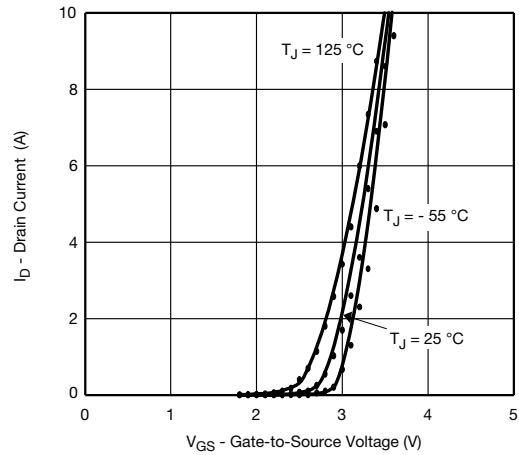
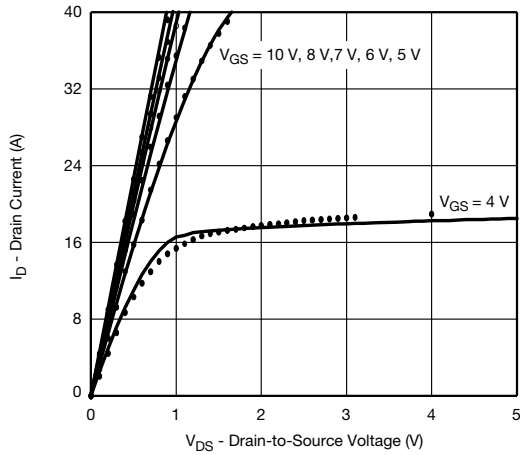


Note

Dots and squares represent measured data.

COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)

P-Channel MOSFET



Note

Dots and squares represent measured data.



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