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P-Channel 30 V (D-S) 175 °C MOSFET

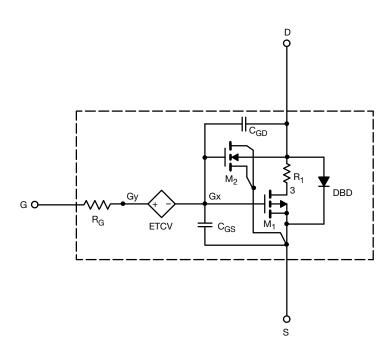
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - $55\,^{\circ}\text{C}$ to + $125\,^{\circ}\text{C}$ temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



SPICE Device Model SQ4431EY

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| SPECIFICATIONS T _J = 25 °C, unless otherwise noted | | | | | |
|--|---------------------|--|----------------|------------------|------|
| PARAMETER | SYMBOL | TEST CONDITIONS | SIMULATED DATA | MEASURED DATA | UNIT |
| Static | | | | | |
| Gate-Source Threshold Voltage | V _{GS(th)} | $V_{DS} = V_{GS}, I_{D} = -250 \mu A$ | 2 | - | V |
| Drain-Source On-State Resistance ^a | R _{DS(on)} | V _{GS} = - 10 V, I _D = - 6 A | 0.021 | 0.020 | Ω |
| | | V _{GS} = - 4.5 V, I _D = - 5 A | 0.040 | 0.039 | |
| Forward Transconductance ^a | 9 _{fs} | V _{DS} = - 15 V, I _D = - 6 A | 12 | 15 | S |
| Diode Forward Voltage | V _{SD} | I _S = - 2.1 A | - 0.80 | - 0.80 | V |
| Dynamic ^b | | | | | |
| Input Capacitance | C _{iss} | V _{DS} = - 15 V, V _{GS} = 0 V, f = 1 MHz | 1010 | 1010 | pF |
| Output Capacitance | C _{oss} | | 242 | 243 | |
| Reverse Transfer Capacitance | C _{rss} | | 156 | 167 | |
| Total Gate Charge | Qg | V _{DS} = - 15 V, V _{GS} = - 10 V, I _D = - 7.2 A | 21 | 25 | nC |
| Gate-Source Charge | Q _{gs} | | 4 | 4 | |
| Gate-Drain Charge | Q_{gd} | | 5 | 5 | |

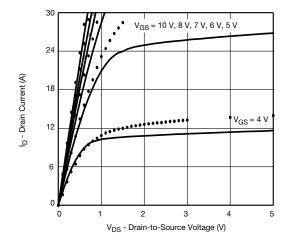
Notes

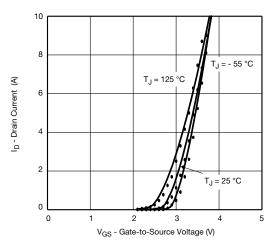
- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

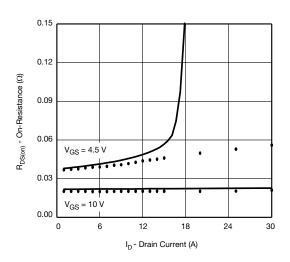
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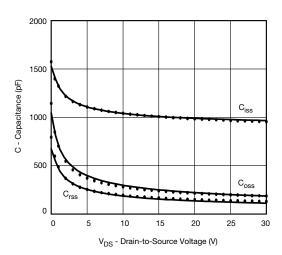
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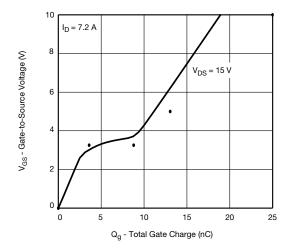
COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25~{}^{\circ}\text{C}$, unless otherwise noted

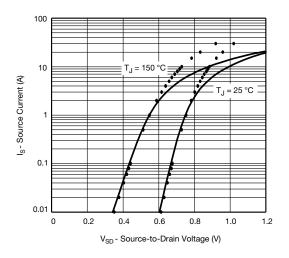












Note

• Dots and squares represent measured data.



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