

Vishay Siliconix

### N-Channel 100 V (D-S) 175 °C MOSFET

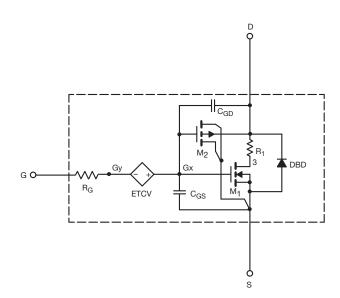
#### **DESCRIPTION**

The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -  $55\,^{\circ}\text{C}$  to +  $125\,^{\circ}\text{C}$  temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### SUBCIRCUIT MODEL SCHEMATIC

#### **CHARACTERISTICS**

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics



#### Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

## SPICE Device Model SQM47N10-24L

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<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.7	-	V
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, I_D = 40 \text{ A}$	0.016	0.017	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$	0.019	0.020	
Forward Transconductancea	9 <sub>fs</sub>	$V_{DS} = 15 \text{ V}, I_D = 40 \text{ A}$	68	85	S
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 40 A	0.85	0.85	V
Dynamic <sup>b</sup>					
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz	2900	2893	pF
Output Capacitance	C <sub>oss</sub>		315	321	
Reverse Transfer Capacitance	C <sub>rss</sub>		122	126	
Total Gate Charge	$Q_g$	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40 A	48	48	nC
Gate-Source Charge	Q <sub>gs</sub>		10	10	
Gate-Drain Charge	$Q_{gd}$		10	10	

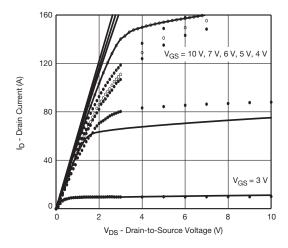
#### Notes

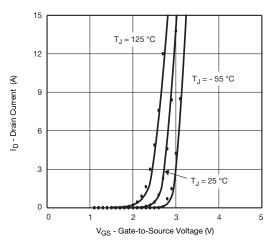
- a. Pulse test; pulse width  $\leq 300~\mu s,\,duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

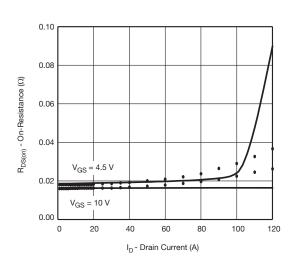


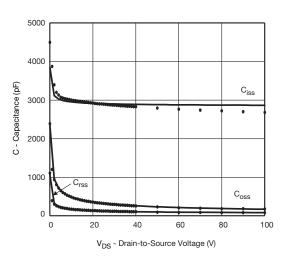
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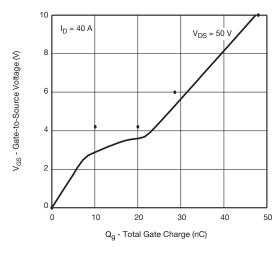
### **COMPARISON OF MODEL WITH MEASURED DATA** ( $T_J = 25$ °C, unless otherwise noted)

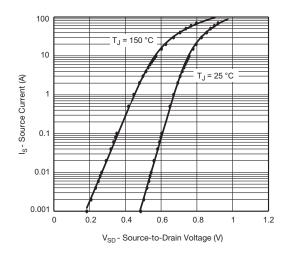












#### Note

• Dots and squares represent measured data.



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