

Vishay Siliconix

N-Channel 200 V (D-S) MOSFET

DESCRIPTION

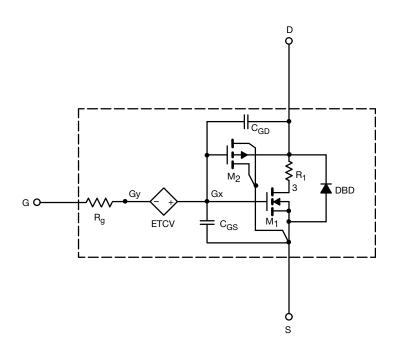
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 $^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$ temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- · Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	3	-	V
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_{D} = 10 \text{ A}$	0.041	0.042	Ω
		$V_{GS} = 7.5 \text{ V}, I_D = 10 \text{ A}$	0.043	0.043	
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 15 \text{ V}, I_{D} = 10 \text{ A}$	22	35	S
Diode Forward Voltage	V _{SD}	I _S = 5 A	0.80	0.81	V
Dynamic ^b					
Input Capacitance	C _{iss}	V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz	1460	1450	pF
Output Capacitance	C _{oss}		117	116	
Reverse Transfer Capacitance	C _{rss}		22	9	
Total Gate Charge	Qg	V _{DS} = 100 V, V _{GS} = 10 V, I _D = 10 A	23.4	23.7	nC
		V _{DS} = 100 V, V _{GS} = 7.5 V, I _D = 10 A	18.3	18.3	
Gate-Source Charge	Q _{gs}		6.3	6.3	
Gate-Drain Charge	Q _{gd}		6	6	

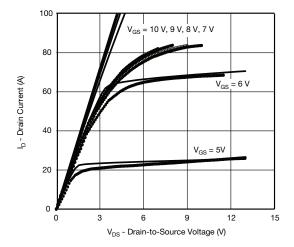
Notes

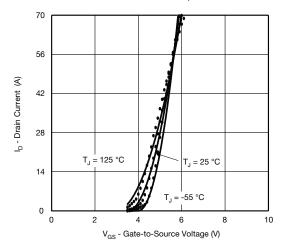
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

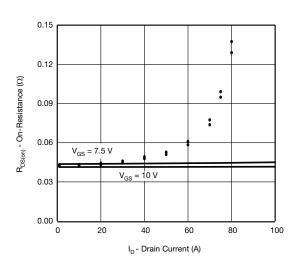
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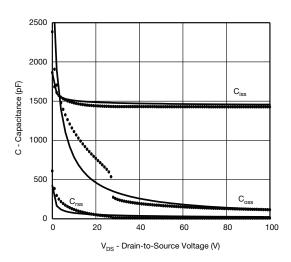
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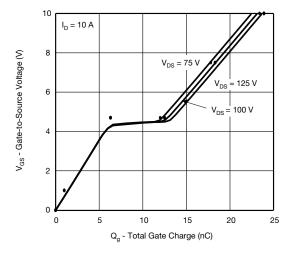
COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25$ °C, unless otherwise noted)

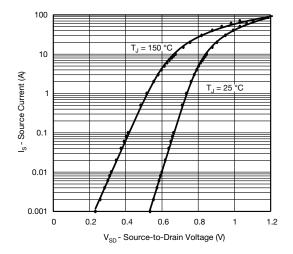












Note

Dots and squares represent measured data.
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