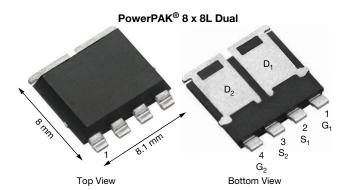
SQJQ904E

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SHA

Vishay Siliconix

Automotive Dual N-Channel 40 V (D-S) 175 °C MOSFET



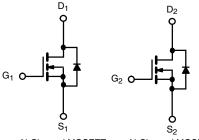
PRODUCT SUMMARY	
V _{DS} (V)	40
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 V$	0.0034
I _D (A) per leg	100
Configuration	Dual
Package	PowerPAK 8 x 8L

FEATURES

- TrenchFET[®] power MOSFET
- AEC-Q101 qualified
- 100 % R_q and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



RoHS COMPLIANT HALOGEN FREE



N-Channel MOSFET N-Channel MOSFET

ABSOLUTE MAXIMUM RATING	S (T _C = 25 °C, unles	s otherwise noted	l)	
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V _{DS}	40	V
Gate-source voltage		V _{GS}	± 20	v
Continuous drain current	T _C = 25 °Ca	I-	100	
Continuous drain current	T _C = 125 °C	ID	64	
Continuous source current (diode conductio	n) ^a	I _S	100	А
Pulsed drain current ^b		I _{DM}	300	
Single pulse avalanche current	L = 0.1 mH	I _{AS}	50	
Single pulse avalanche energy		E _{AS}	125	mJ
Maximum power dissipation ^b	T _C = 25 °C	P	75	W
Maximum power dissipation -	T _C = 125 °C	PD	25	vv
Operating junction and storage temperature	range	T _J , T _{stg}	-55 to +175	°C
Soldering recommendations (peak temperat	ure) ^{d, e}		260	C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount ^c	R _{thJA}	85	°C/W
Junction-to-case (drain)		R _{thJC}	2	0/10

Notes

a. Package limited.

b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

c. When mounted on 1" square PCB (FR4 material).

d. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK 8 x 8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

1

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PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static	·	·					
Drain-source breakdown voltage	V _{DS}	V _{GS}	= 0, I _D = 250 μA	40	-	-	v
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	- V _{GS} , I _D = 250 μA	2.5	3	3.5	v
Gate-source leakage	I _{GSS}	V _{DS} =	0 V, $V_{GS} = \pm 20 V$	-	-	± 100	nA
		$V_{GS} = 0 V$	V _{DS} = 20 V	-	-	1	
Zero gate voltage drain current	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 40 V, T _J = 125 °C	-	-	50	μA
		$V_{GS} = 0 V$	$V_{DS} = 40 \text{ V}, \text{ T}_{J} = 175 ^{\circ}\text{C}$	-	-	150	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	40	-	-	Α
		$V_{GS} = 10 V$	I _D = 20 A	-	0.0029	0.0034	Ω
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = 10 V$	$I_D = 20 \text{ A}, \text{T}_\text{J} = 125 \ ^\circ\text{C}$	-	-	0.0074	
		V _{GS} = 10 V	I _D = 20 A, T _J = 175 °C	-	-	0.0091	
Forward transconductance ^b		V _{DS} = 15 V, I _D = 15 A		-	80	-	S
Dynamic ^b							
Input capacitance	C _{iss}			-	4530	5900	
Output capacitance	C _{oss}	$V_{GS} = 0 V$	V _{DS} = 20 V, f = 1 MHz	-	2750	3300	pF
Reverse transfer capacitance	C _{rss}			-	168	220	
Total gate charge ^c	Qg			-	60	75	
Gate-source charge ^c	Q _{gs}	$V_{GS} = 10 V$	$V_{DS} = 20 \text{ V}, I_D = 40 \text{ A}$	-	16	-	nC
Gate-drain charge ^c	Q _{gd}	1		-	5	-	
Gate resistance	Rg	f = 1 MHz		0.5	1	2	Ω
Turn-on delay time ^c	t _{d(on)}			-	15.5	20	
Rise time ^c	t _r	V _{DD} =	= 20 V, $R_{\rm L}$ = 0.5 Ω	-	4.6	6.2	
Turn-off delay time ^c	t _{d(off)}		$V_{\text{GEN}} = 10 \text{ V}, \text{ R}_{\text{g}} = 1 \Omega$	-	30	38	ns
Fall time ^c	t _f	1		-	4	7	
Source-Drain Diode Ratings and Cha	racteristics ^b						
Pulsed current ^a	I _{SM}			-	-	200	Α
Puised current "	ISM					200	<i>.</i> .

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

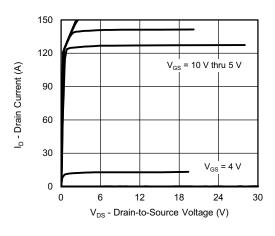
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

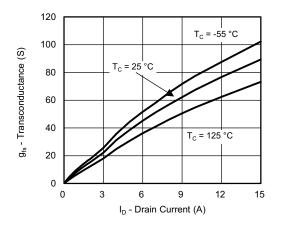
2



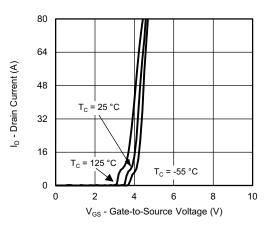
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



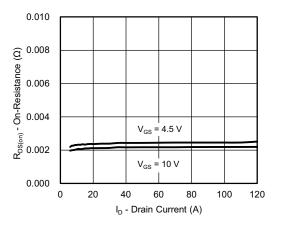
Output Characteristics



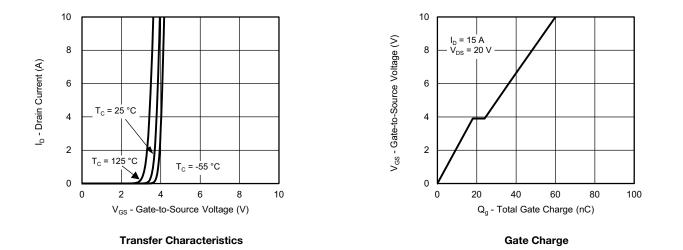
Transconductance



Transfer Characteristics



On-Resistance vs. Drain Current



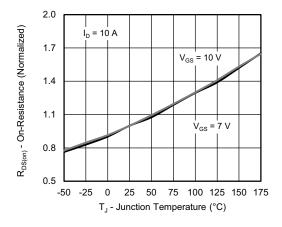
S17-0256-Rev. A, 20-Feb-17

3 ns. contact: automostechs Document Number: 68442

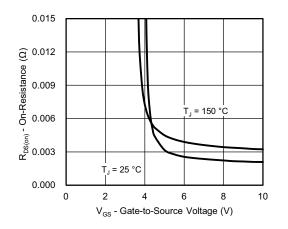
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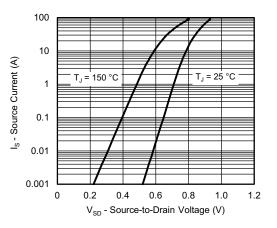
TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)



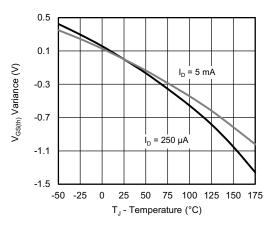
On-Resistance vs. Junction Temperature

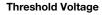


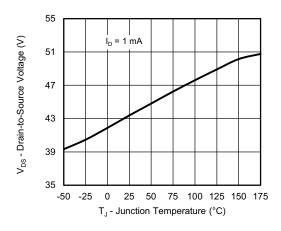
On-Resistance vs. Gate-to-Source Voltage



Source Drain Diode Forward Voltage







Drain Source Breakdown vs. Junction Temperature

4

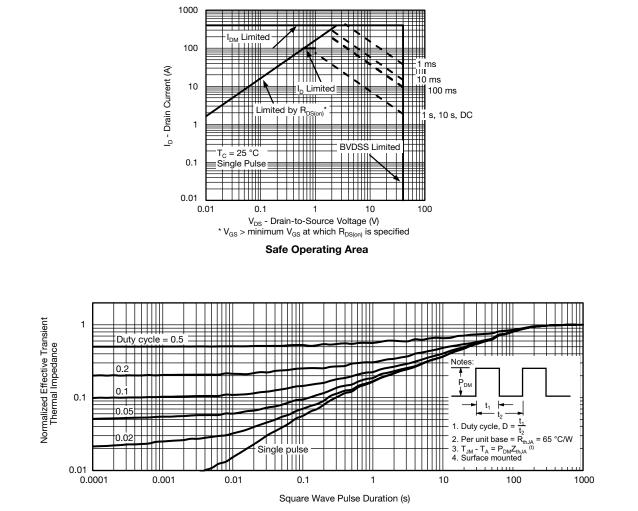
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SQJQ904E

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THERMAL RATINGS ($T_A = 25 \text{ °C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

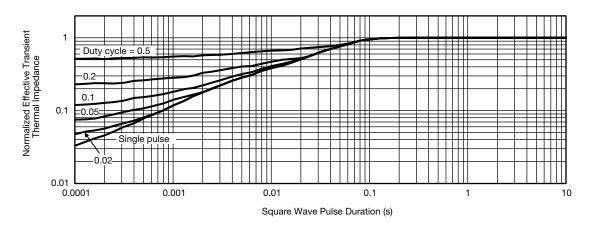


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Document Number: 68442

THERMAL RATINGS ($T_A = 25 \text{ °C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

• The characteristics shown in the two graphs

S17-0256-Rev. A, 20-Feb-17

- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

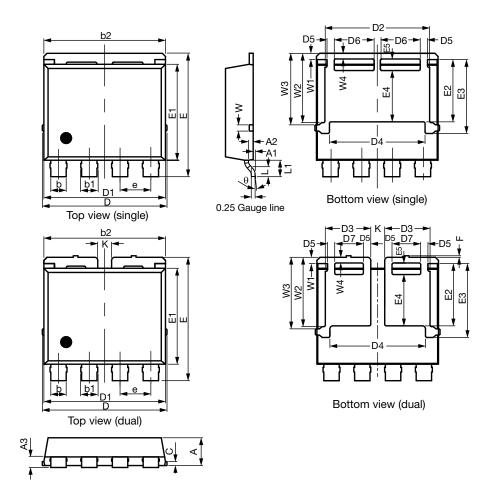
- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68442.







DIM.		MILLIMETERS		INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
А	1.70	1.80	1.90	0.067	0.071	0.075	
A1	0.00	0.08	0.13	0.000	0.003	0.005	
A2	0.25	0.30	0.35	0.010	0.012	0.014	
A3	0.55	0.62	0.70	0.022	0.024	0.028	
b	0.92	1.00	1.08	0.036	0.039	0.043	
b1	1.02	1.10	1.18	0.040	0.043	0.046	
b2	7.80	7.90	8.00	0.307	0.311	0.315	
С	0.20	0.25	0.30	0.008	0.010	0.012	
D	8.00	8.10	8.25	0.315	0.319	0.325	
D1	7.80	7.90	8.00	0.307	0.311	0.315	
D2	6.70	6.80	6.90	0.264	0.268	0.272	
D3	2.85	2.95	3.05	0.112	0.116	0.120	
D4	6.11	6.21	6.31	0.241	0.244	0.248	
D5	0.37	0.47	0.57	0.015	0.019	0.022	
D6	2.49	2.59	2.69	0.098	0.102	0.106	
D7	1.76	1.86	1.96	0.069	0.073	0.077	

Revision: 16-Oct-17

Document Number: 67734

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Package Information



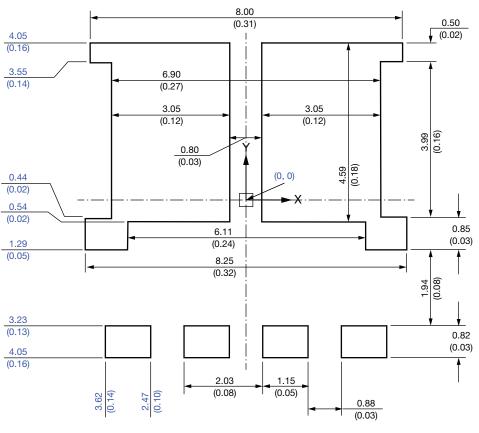


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DIM.	MILLIMETERS			INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
е	1.95	2.00	2.05	0.077	0.079	0.081	
Е	7.90	8.00	8.10	0.311	0.315	0.319	
E1	6.12	6.22	6.32	0.241	0.245	0.249	
E2	3.94	4.04	4.14	0.140	0.159	0.163	
E3	4.69	4.79	4.89	0.185	0.189	0.193	
E4	3.23	3.33	3.43	0.127	0.131	0.135	
E5	0.65	0.75	0.85	0.026	0.030	0.033	
F	0.00	0.10	0.15	0.000	0.004	0.006	
L	0.62	0.72	0.82	0.024	0.028	0.032	
L1	0.92	1.07	1.22	0.036	0.042	0.048	
К	0.80	0.90	1.00	0.031	0.035	0.039	
W	0.30	0.40	0.50	0.012	0.016	0.020	
W1	0.30	0.40	0.50	0.012	0.016	0.020	
W2	4.39	4.49	4.59	0.173	0.177	0.181	
W3	4.54	4.64	4.74	0.179	0.183	0.187	
W4	0.32	0.37	0.42	0.013	0.015	0.017	
θ	6°	10°	14°	6°	10°	14°	



Recommended Minimum PADs for PowerPAK® 8 x 8L Dual



Dimensions in millimeters (inches)

Note

• Linear dimensions are in black, the same information is provided in ordinate dimensions which are in blue.



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1