**Power MOSFETs** 

Application Note 835

## PCB Design and Surface-Mount Assembly Guidelines for MICRO FOOT® Packages

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#### Introduction

The Vishay Siliconix MICRO FOOT® product family is based on wafer-level chip scale packaging (WL-CSP) technology that implements a solder bump process to eliminate the need for an outer package to encase the silicon die. MICRO FOOT products include power MOSFETs, analog switches, and power ICs.

For portable devices, this new packaging technology reduces board space requirements, improves thermal performance, and mitigates the parasitic effect typical of leaded package products. For example, the 6 bump MICRO FOOT Si8902EDB common-drain power MOSFET, which measures just 1.6 mm by 2.4 mm, achieves the same performance as TSSOP-8 devices in a footprint that is 80 % smaller and with a 50 % lower profile (figure 1). A MICRO FOOT analog switch, the 6 bump DG3000DB, offers low charge injection and 1.4  $\Omega$  on-resistance in a footprint measuring just 1.08 mm by 1.58 mm (figure 2).



Figure 1. 3D View of MICRO FOOT Si8902EDB and TSSOP-8

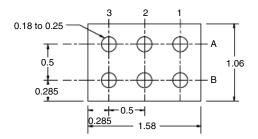


Figure 2. Outline of MICRO FOOT CSP and DG3000DB Analog Switch

MICRO FOOT products can be handled with the same process techniques used for high-volume assembly of packaged surface-mount devices. With proper attention to PCB and stencil design, the devices will achieve reliable performance without underfill. The advantage of the devices' small footprints and short thermal paths make them ideal options for space-constrained applications in portable devices such as battery packs, PDAs, cellular phones, MP3 players, and notebook computers.

This application note discusses the mechanical structure and reliability of MICRO FOOT products, and provides guidelines for handling, board layout, the assembly process, and the PCB rework process.

#### **MICRO FOOT's Structure and Reliability**

#### **MICRO FOOT Structure**

The MICRO FOOT structure is built upon a silicon wafer substrate. A silicon nitride passivation layer is applied to the active area as the last masking process in wafer fabrication, ensuring that the finished devices pass the moisture-resistance stressing qualification. Laser marking is used to mark the backside of the die. Figure 3 shows the typical dimensions of a MICRO FOOT Si8441DB. Table 1 shows the main parameters for solder bumps used in MICRO FOOT products.

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Figure 3. Typical Dimensions of MICRO FOOT Si8441DB

TABLE 1 - MAIN PARAMETERS OF SOLDER BUMPS IN MICRO FOOT DEVICES						
MICRO FOOT CSP	BUMP PITCH (mm)	BUMP DIAMETER (mm)	BUMP HEIGHT (mm)	BUMP MATERIAL		
MICRO FOOT CSP MOSFET	0.80	0.37 to 0.41	0.26 to 0.29	- Eutectic Solder:		
MICRO FOOT CSP MOSFET	0.50	0.32 to 0.34	0.21 to 0.24	63 Sn/37 Pb;		
MICRO FOOT CSP MOSFET	0.40	0.18 to 0.25	0.14 to 0.19	or		
MICRO FOOT CSP Analog Switch	0.50	0.18 to 0.25	0.14 to 0.19	Lead (Pb)-free Solder:		
MICRO FOOT UCSP Analog Switch	0.50	0.32 to 0.34	0.21 to 0.24	Sn 95.5, Ag 3.6, Cu 0.7		

#### **MICRO FOOT Reliability Test Data**

MICRO FOOT products are qualified for up to three reflow operations (+ 260 °C peak), per J-STD-020.

The main failure mechanism associated with WL-CSP is thermal fatigue of the solder joint. The results shown in table 2 demonstrate that a high level of reliability can be achieved with proper board design and assembly techniques. These reliability results are for MICRO FOOT products mounted on FR-4 boards without underfill.

TABLE 2 - MICRO FOOT RELIABILITY RESULTS							
REL TEST	REL TEST TEST CONDITIONS ACCEPTANCE CRITERIA		JEDEC STANDARDS				
	0	0.8 mm	> 325 g				
Solder Ball Shear Test	Constant shear speed; 50 µm above the pad surface	0.5 mm	> 300 g	JESD22-B117			
	the pad duriade	0.4 mm	> 280 g				
Thermal Cycle Test	Condition B: - 55 °C - 125 °C	1000 cycles		JESD22-A104-A			
Pressure Pot Test	121 °C, 100 % RH, 15 psig	96 h		JESD22-A102-B			
HAST: Highly Accelerated Temperature and Humidity Stress	130 °C, 85 % RH	100 h		JESD22-A110-B			
High Temperature Operating Life Test	150 °C, max. spec. current density	1000 h		JESD22-A108-A			



### PCB Design and Surface-Mount Assembly Guidelines for MICRO FOOT® Packages

#### **MICRO FOOT Carrier Tape**

Fully tested and inspected MICRO FOOT devices are supplied in 8 mm wide or 12 mm wide embossed carrier tape in accordance with standard EIA/IS-763. Figure 4 illustrates an example of the carrier tape for MICRO FOOT products, while table 3 shows the dimension information of some carrier tapes used in MICRO FOOT parts. The devices are placed in the pocket of the carrier tape in a bumps-down orientation in order to facilitate pickup by the component placement machine. The carrier tape is designed so that the component does not rotate more than  $\pm$  5°, nor does it exhibit a lateral movement of more than 0.3 mm, eliminating the need to inspect the component location before pickup. During the component taping operation, every device undergoes an automatic optical inspection that checks for the correct application of the solder balls to the device.

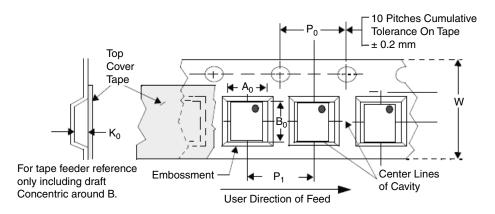


Figure 4. Carrier Tape and Dimension Information

TABLE 3 - CARRIER TAPE AND DIMENSION INFORMATION FOR SELECT MICRO FOOT PARTS									
MICRO FOOT CHIP SIZE		SOLDER BALL		POCKET SIZE (mm)	TAPE	REEL	QUANTITY	D	P <sub>1</sub>
PART #	(mm)	BALL PITCH	BALL ARRAY	$B_0 \times A_0 \times K_0$	WIDTH	DIAMETER	(UNIT)	P <sub>0</sub>	P1
Si8401DB	1.50 x 1.50	0.80 mm	2 x 2	1.71 x 1.71 x 0.81	8.0 mm	178 mm	3500	4.0 mm	4.0 mm
Si8441DB	1.50 x 1.00	0.50 mm	2 x 3	1.63 x 1.13 x 0.78	8.0 mm	178 mm	3500	4.0 mm	4.0 mm
Si8900EDB	4.00 x 2.00	0.80 mm	2 x 5	4.22 x 2.21 x 0.81	12.0 mm	178 mm	3500	4.0 mm	4.0 mm
Si8902EDB	2.40 x 1.60	0.80 mm	2 x 3	2.64 x 1.88 x 0.91	12.0 mm	178 mm	3500	4.0 mm	4.0 mm

#### **PCB Layout Guidelines**

#### **Board Materials**

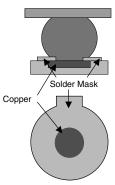
MICRO FOOT packages are designed to be reliable on most board types, including organic boards such as FR-4 or polyamide. The package qualification information is based on tests of 0.5 oz FR-4 and polyamide boards with non-solder mask defined (NSMD) pad designs.

#### **Land Patterns**

Two types of land patterns are used for surface-mount packages. Solder mask defined (SMD) pads have a solder mask opening that is smaller than the metal pad (see figure 5). NSMD pads have a metal pad that is smaller than the solder mask opening (figure 6).

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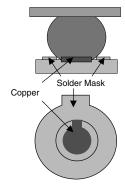


Figure 5. SMD

Figure 6. NSMD

NSMD pads are recommended for copper etch processes, since they provide a higher level of process control compared to SMD etch processes. A small-size NSMD pad definition provides more areas (both lateral and vertical) for soldering and more room for escape routing on the PCB. By contrast, SMD pad definition introduces a stress concentration point near the solder mask on the PCB side that may result in solder join cracking under extreme-fatigue conditions.

#### **Board Pad Design**

A copper layer thickness of less than 1 oz. is recommended to achieve higher standoff. A 1 oz. ( $\sim$ 30  $\mu$ m) or greater copper thickness results in a lowering of the effective standoff, which may compromise solder joint reliability.

Copper pads should be finished with organic surface preservative coating (OSP). For electroplated nickel-immersion gold finish pads, the gold thickness must be less than 0.2 µm to avoid solder joint embrittlement.

For the NSMD pad geometry, the trace width at the connection to the land pad should not exceed 67 % of the pad diameter.

For PCB layouts employing via-in pad structures (microvia), NSMD pad definition should be used, since this ensures an adequate wetting area on the copper pads, and hence a better joint. It is recommended that the wall thickness of the microvias be a minimum of 15  $\mu$ m. It is recommended that 'offset' vias be used when microvias are required for routing on the PCB.

The fan-out for the traces should be symmetrical across the X and Y directions to avoid part rotation due to the surface tension of molten solder. Hot air solder leveled (HASL) board finish is not recommended.

The landing pad size for MICRO FOOT products is determined by the bump pitch, as shown in table 4. The pad pattern is in a circle shape to ensure a symmetric, barrel-shaped solder bump.

TABLE 4 - DIMENSIONS OF COPPER PAD AND SOLDER MASK OPENINGS IN THE PCB							
MICRO FOOT PRODUCTS/PITCH	MOSFET 0.80 mm PITCH		MOSFET AND UCSP ANALOG SWITCH; 0.5 mm PITCH		MOSFET: 0.4 mm PITCH; ANALOG SWITCH: 0.5 mm PITCH		
SOLDER BALL SIZE	Ø 0.37 to 0.41 mm		Ø 0.32 to 0.34 mm		Ø 0.18 to 0.25 mm		
Pad Definition	Copper Pad	Solder Mask Opeing	Copper Pad	Solder Mask Opeing	Copper Pad	Solder Mask Opeing	
NSMD	0.30 ± 0.01 mm	0.41 ± 0.01 mm	0.17 ± 0.01 mm	0.27 ± 0.01 mm	0.17 ± 0.01 mm	0.27 ± 0.01 mm	
SMD	0.41 ± 0.01 mm	0.30 ± 0.01 mm	0.27 ± 0.01 mm	0.17 ± 0.01 mm	0.27 ± 0.01 mm	0.17 ± 0.01 mm	

#### **Surface-Mount Assembly Process**

The MICRO FOOT products' surface-mount assembly operations include solder paste printing, component placement, and solder reflow. This is shown in the process flow chart in figure 7.

#### **SMT Assembly Process Flow Chart**



Figure 7. Surface-Mount Assembly Process Flow



### PCB Design and Surface-Mount Assembly Guidelines for MICRO FOOT® Packages

#### **Stencil Design**

Stencil design is the key to ensuring maximum solder paste deposition without compromising the assembly yield from solder joint defects, such as bridging, and extraneous solder spheres. The stencil aperture and thickness are dependent on the copper pad size, the solder mask opening, and the quantity of solder paste.

The optimum stencil thickness is 0.125 mm (5 mils) for MICRO FOOT 0.80 mm pitch products, 0.1 mm (4 mils) for MICRO FOOT 0.5 mm pitch MOSFETs, analog switches, UCSP analog switches, and 0.4 mm pitch MOSFET products.

The recommended apertures are shown in table 5 and are fabricated by laser cutting.

TABLE 5 - RECOMMENDED STENCIL APERTURES					
MICRO FOOT	MOSFET	MOSFET AND UCSP ANALOG SWITCH	MOSFET: 0.4 mm PITCH		
PRODUCTS/PITCH	0.8 mm PITCH	0.5 mm PITCH	ANALOG SWITCH: 0.5 mm PITCH		
Recommended Stencil	0.33 ± 0.01 mm in Circle	0.30 ± 0.01 mm in Circle	0.38 ± 0.01 mm in Circle		
Aperture Size	Aperture	Aperture	Aperture		

#### **Solder Paste Printing**

The solder paste printing process involves transferring solder paste through pre-defined apertures via the application of pressure. The solder paste recommended is eutectic 63Sn/37Pb no-clean solder paste or lead (Pb)-free 95.5Sn3.8Ag0.7Cu no-clean solder paste. Stencil alignment accuracy should be  $\pm$  50  $\mu m$ . It is recommended to use type 3 (25  $\mu m$  to 45  $\mu m$  particle size range) or fine solder paste for printing.

Solder paste printing parameters should be optimized using standard procedures for specific printing machines to ensure repeatable deposits for all the pads on the entire board

It is very important to clean the stencil frequently during printing operations, preferably after every application or every other application. Dry clean the stencils as often as possible; wet cleaning should be avoided if possible. This will help to minimize printing defects, especially from the paste or residue at the bottom of the stencil.

#### **Chip Pick and Placement**

MICRO FOOT parts can be picked up from pocketed carrier tape reels and placed directly onto PCBs with standard pick-and-process equipment.

A non-metallic pickup tool (nozzle) should be used to avoid scratching the top surface of the device, which could result in nucleation sites for microcracking.

The side-lighting option on the pick-and-place machine's vision system should be used when attempting to use an individual bump recognition approach to ensure greater clarity in bump recognition.

Feeders should be well maintained to eliminate any sources of vibration since feed vibration can cause misalignment or complete dislocation of the devices within the pocket after the cover tape has been peeled back.

Extreme care should be used when any tool comes into contact with the devices. The silicon chip is made of glass, and can easily be subject to damage. To prevent die cracking during pickup and placement, the pick-and-place force should be less than 150 g during pickup. No force needs to be exerted during placement. It is recommended that bumps be dipped into solder paste on the PCB to greater than 20 % of the paste block height.

Though the part will self-center during solder reflow, the maximum placement offset is 0.02 mm.

#### **Reflow Process**

MICRO FOOT products are compatible with all industry solder reflow processes for both Eutectic and Pb-free processes. Nitrogen purge is recommended during reflow operation to ensure optimum solderability.

Figure 8 shows the typical Eutectic/lead (Pb)-free reflow profile. It is comprised of four stages:

- Preheat: From ambient through the first thermal excursion
- Preflow: This portion determines the ramp-up time from the preheat temperature to the reflow temperature
- Reflow (wetting): This portion determines the time of the actual reflow. The minimum peak temperature (T<sub>P</sub>) needs to exceed the melting point of the alloy
- Cooldown: After the peak temperatures are attained, the PCB passes out of the heated portion of the reflow oven.
  The cooling rates should not exceed - 4 °C/s



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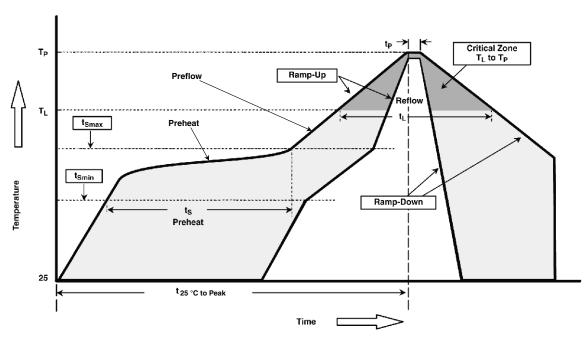


Figure 8. Lead (Pb)-free/Eutectic Ramp or Tent Reflow Profile

Table 6 shows the main reflow parameters used in Eutectic 37Pb63Pb and lead (Pb)-free solder alloys.

TABLE 6 - MAIN REFLOW PARAMETERS FOR EUTECTIC AND LEAD (Pb)-FREE REFLOW PROFILES					
	PROFILE FEATURE	EUTECTIC 63_Sn 37_Pb	LEAD (Pb)-FREE		
	Temp. min. (T <sub>smin</sub> )	100 °C	150 °C		
Preheat	Temp. max. (T <sub>smax</sub> )	150 °C	200 °C		
	Time (min. to max.) (t <sub>s</sub> )	60 s to 120 s	60 s to 180 s		
Ramp-up Rate	e (T <sub>smax</sub> to T <sub>L</sub> )	3 °C/s max.	3 °C/s max.		
Melt Temperat	ure (T <sub>L</sub> )	183 °C	217 °C		
Peak Tempera	ture (T <sub>P</sub> )	240 °C	260 °C		
Reflow (Wettir	ng) Time (t <sub>L</sub> )	60 s to 150 s	60 s to 150 s		
Ramp-down F	ate	6 °C/s max.	6 °C/s max.		
Time + 250 °C	to T <sub>P</sub>	6 minutes max.	6 min max.		

#### Flux Cleaning

MICRO FOOT products are compatible with all standard post-solder cleaning processes, including heated water, saponifiers, and solvents. No special cleaning techniques are required due to the small area and large standoff of these devices.

#### **Solder Joint Inspection**

Visual inspection or microscope checks can confirm the ball alignment and tilting. X-ray inspection may be used to detect non-visible solder joints defects such as voiding, ball bridging, and missing balls. Die shear testing may be used to verify the solder joint quality. Table 7 shows the die shear specifications for MICRO FOOT products.



### PCB Design and Surface-Mount Assembly Guidelines for MICRO FOOT® Packages

TABLE 7 - DIE SHEAR SPECIFICATIONS FOR MICRO FOOT PRODUCTS						
MICRO FOOT PRODUCTS	BALL ARRAY	DIE SHEAR SPEC. (kg)				
0.8 mm Pitch MOSFET	2 x 2	1.50				
	2 x 3	1.80				
0.5 mm Pitch MOSFET/	2 x 2	1.00				
UCSP Analog switch	2 x 3	1.20				
0.5 mm Pitch Analog Switch/	2 x 2	1.00				
0.4 mm Pitch MOSFET	2 x 3	1.20				

#### Rework

To replace MICRO FOOT products on the PCB, the rework procedure is much like the rework process for a standard BGA or CSP, as long as the rework process duplicates the original reflow profile. The key steps are as follows:

- 1. Remove the MICRO FOOT device using a convection nozzle to create localized heating similar to the original reflow profile. Preheat from the bottom.
- 2. Once the nozzle temperature is + 190 °C, use tweezers to remove the part to be replaced.
- 3. Resurface the pads using a temperature-controlled soldering iron.
- 4. Apply gel flux to the pad.
- 5. Use a vacuum needle pick-up tip to pick up the replacement part, and use a placement jig to place it accurately.
- 6. Reflow the part using the same convection nozzle and preheat from the bottom, matching the original reflow profile.