Dual N-Channel 20 V (D-S) 175 °C MOSFET

DESCRIPTION

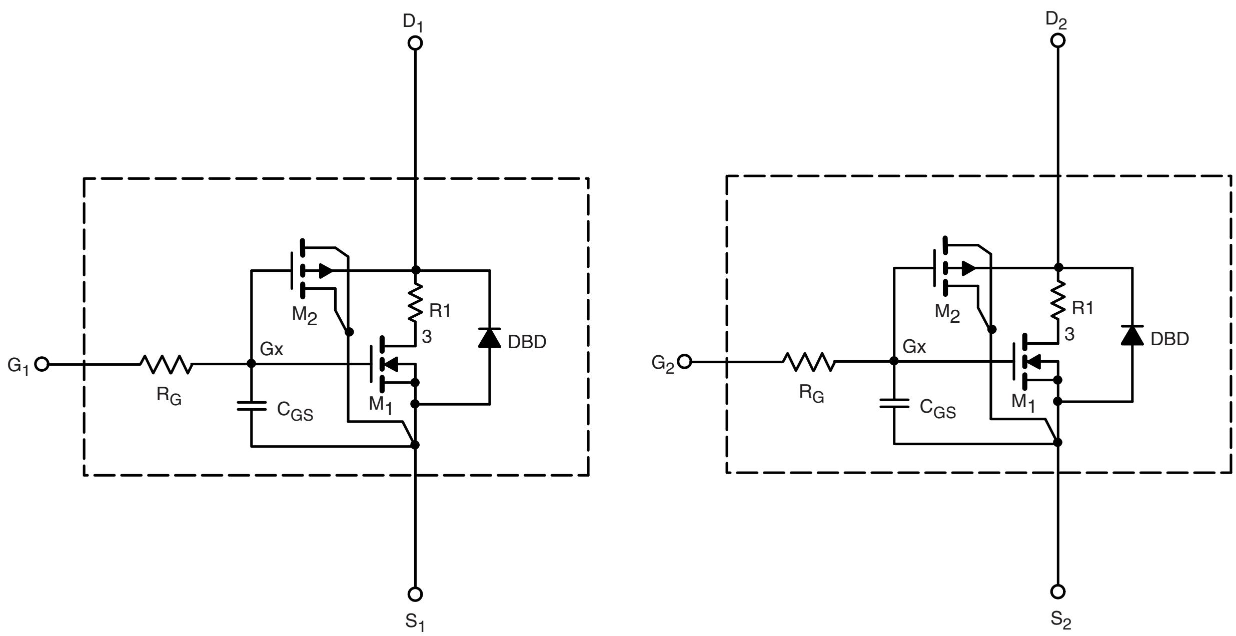
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- Model the gate charge

SUB-CIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

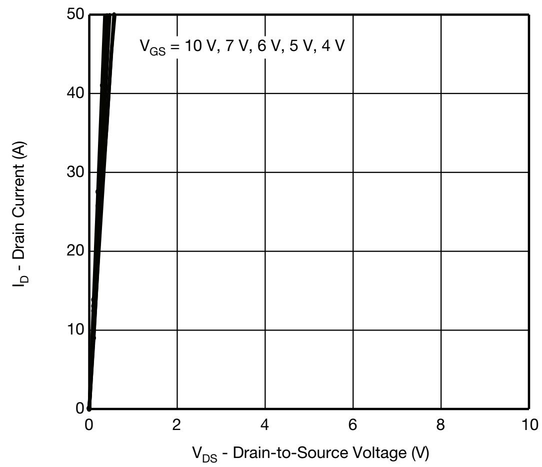
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**CHANNEL**	**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA	N-Ch 1	1.6	1.5	V
			N-Ch 2	1.6	1.5	
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 16 A	N-Ch 1	0.0072	0.0074	Ω
		V_{GS} = 10 V, I_D = 20 A	N-Ch 2	0.0029	0.0031	
		V_{GS} = 4.5 V, I_D = 14 A	N-Ch 1	0.0098	0.0095	
		V_{GS} = 4.5 V, I_D = 19 A	N-Ch 2	0.0042	0.0039	
Forward Transconductance [a]	g_{fs}	V_{DS} = 10 V, I_D = 10 A	N-Ch 1	51	55	S
			N-Ch 2	55	60	
Diode Forward Voltage	V_{SD}	I_S = 10 A	N-Ch 1	0.80	0.80	V
		I_S = 20 A	N-Ch 2	0.82	0.08	
Dynamic [b]						
Input Capacitance	C_{iss}	N-Channel 1 V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz N-Channel 2 V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	N-Ch 1	690	723	pF
			N-Ch 2	1960	1937	
Output Capacitance	C_{oss}		N-Ch 1	267	269	
			N-Ch 2	646	655	
Reverse Transfer Capacitance	C_{rss}		N-Ch 1	111	112	
			N-Ch 2	255	264	
Total Gate Charge	Q_g	N-Channel 1 V_{DS} = 10 V, V_{GS} = 10 V, I_D = 20 A N-Channel 2 V_{DS} = 10 V, V_{GS} = 10 V, I_D = 60 A	N-Ch 1	12	12	nC
			N-Ch 2	30	29	
Gate-Source Charge	Q_{gs}		N-Ch 1	1.6	1.6	
			N-Ch 2	4.1	4.1	
Gate-Drain Charge	Q_{gd}		N-Ch 1	2.5	2.5	
			N-Ch 2	6	6	

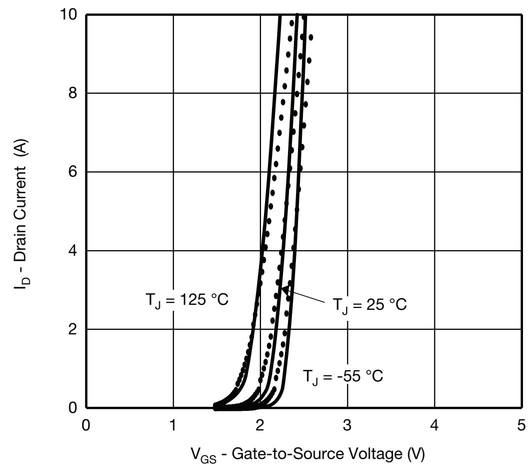
Notes

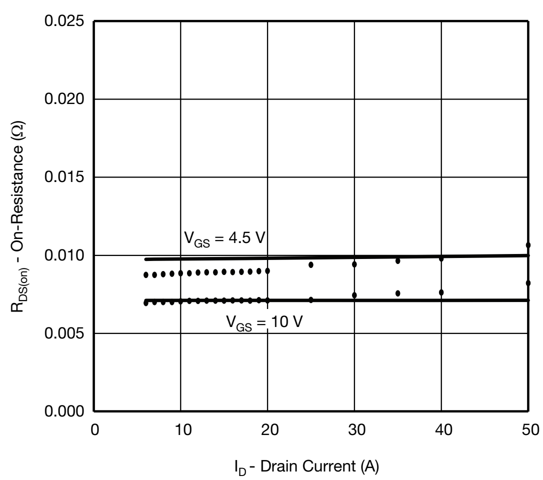
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.

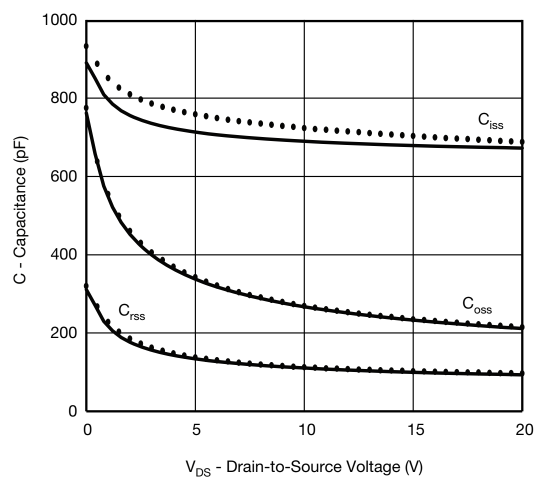
b. Guaranteed by design, not subject to production testing.

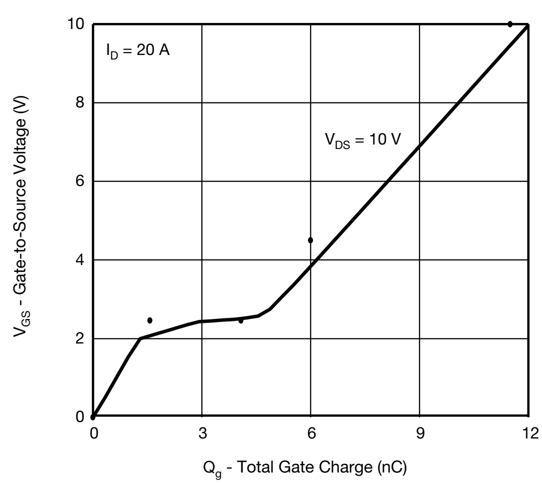
COMPARISON OF MODEL WITH MEASURED DATA N-CHANNEL 1 (T_J = 25 °C, unless otherwise noted)

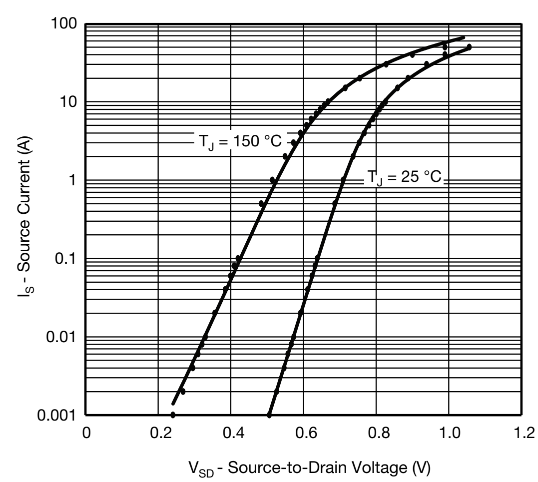








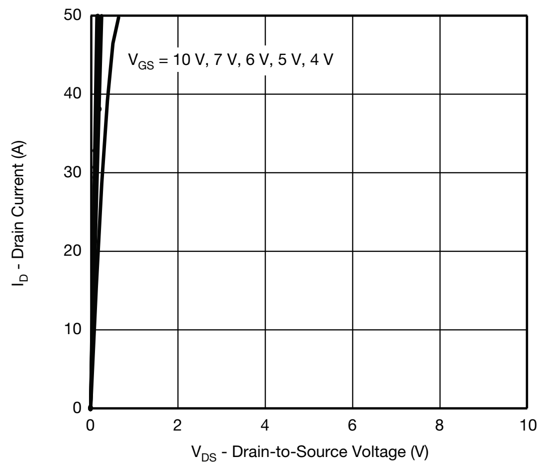


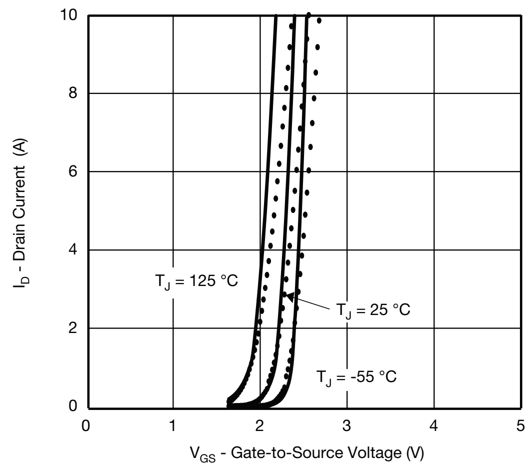


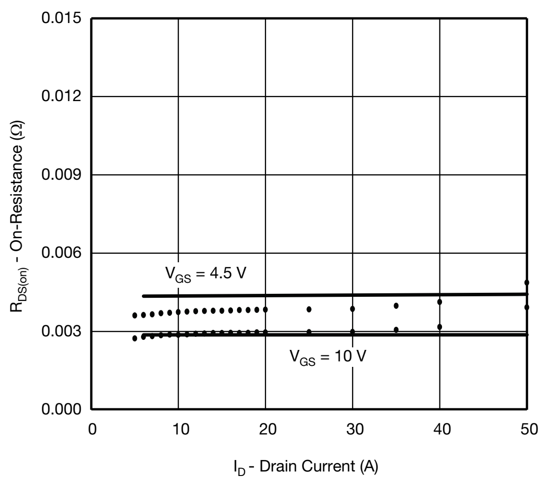
Note

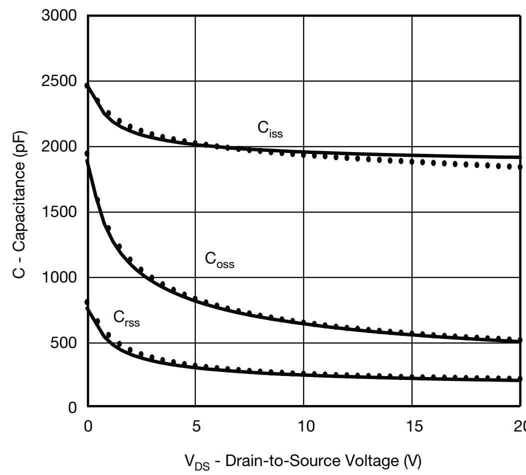
- Dots and squares represent measured data.

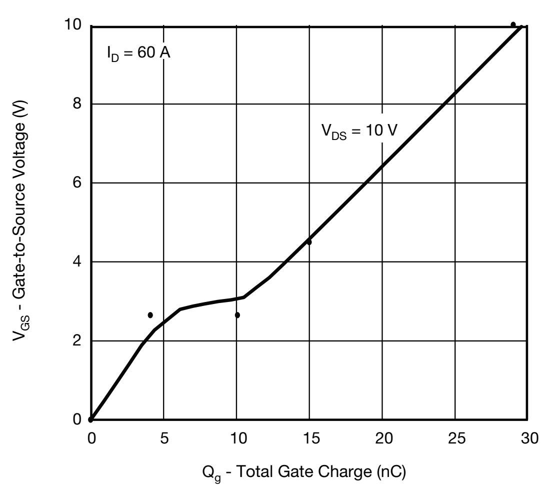
COMPARISON OF MODEL WITH MEASURED DATA N-CHANNEL 2 (T_J = 25 °C, unless otherwise noted)

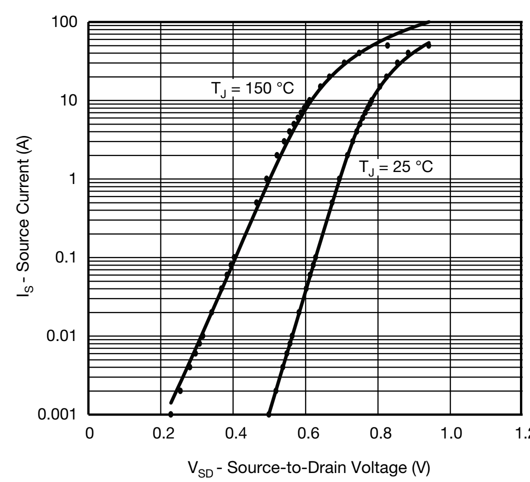












Note

- Dots and squares represent measured data.

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