



### Complementary N- and P-Channel 40-V (D-S) MOSFET

#### CHARACTERISTICS

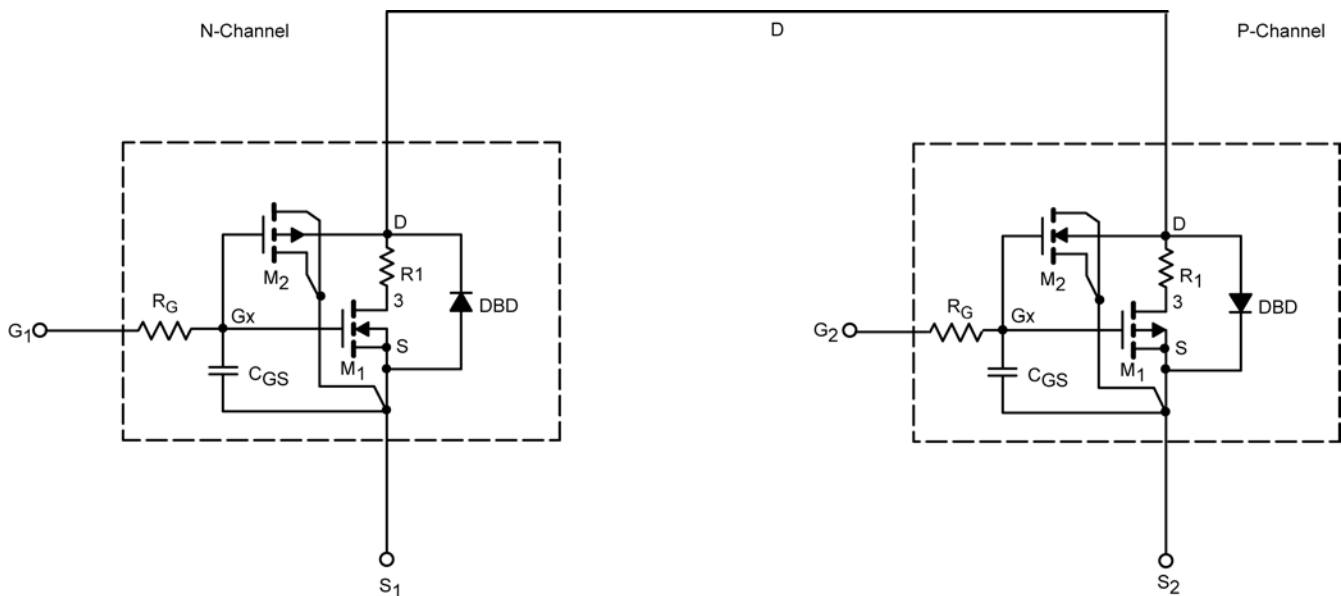
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

#### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T <sub>J</sub> = 25°C UNLESS OTHERWISE NOTED)								
Parameter	Symbol	Test Condition		Simulated Data	Measured Data	Unit		
<b>Static</b>								
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	1.8		V		
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	P-Ch	1.7				
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5 A	N-Ch	0.029	0.0305	Ω		
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -5 A	P-Ch	0.0283	0.030			
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 4 A	N-Ch	0.0352	0.037			
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -4 A	P-Ch	0.037	0.040			
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 5 A	N-Ch	13	22	S		
		V <sub>DS</sub> = -15 V, I <sub>D</sub> = -5 A	P-Ch	15	20			
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 2 A	N-Ch	0.71	0.80	V		
		I <sub>S</sub> = -2 A	P-Ch	0.76	-0.76			
<b>Dynamic<sup>b</sup></b>								
Input Capacitance	C <sub>iss</sub>	N-Channel V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, f = 1 MHz P-Channel V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V, f = 1 MHz	N-Ch	641	640	pF		
			P-Ch	1593	1555			
Output Capacitance	C <sub>oss</sub>		N-Ch	72	73			
			P-Ch	176	176			
Reverse Transfer Capacitance	C <sub>rss</sub>		N-Ch	34	41			
			P-Ch	131	142			
Total Gate Charge	Q <sub>g</sub>		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5 A	N-Ch	10		11.7	nC
			V <sub>DS</sub> = -20 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -5 A	P-Ch	30		38.5	
		N-Channel V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5 A	N-Ch	5.1	5.3			
			P-Ch	16	17			
Gate-Source Charge	Q <sub>gs</sub>	P-Channel V <sub>DS</sub> = -20 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -5 A	N-Ch	1.9	1.9			
			P-Ch	4.2	4.2			
Gate-Source Charge	Q <sub>gs</sub>		N-Ch	1.7	1.7			
			P-Ch	7	7			

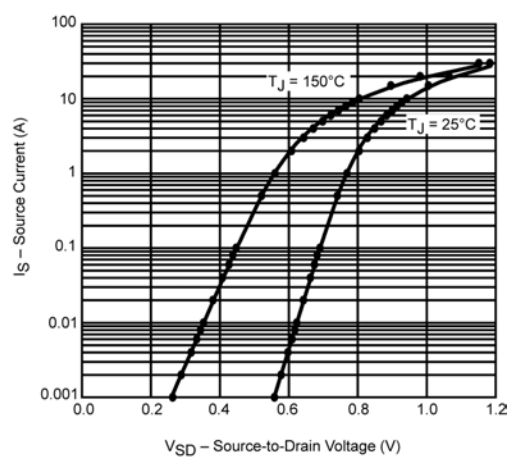
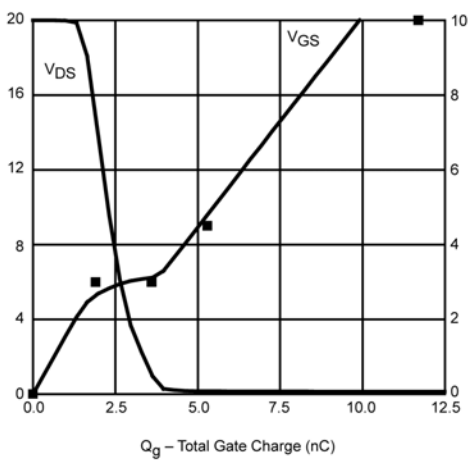
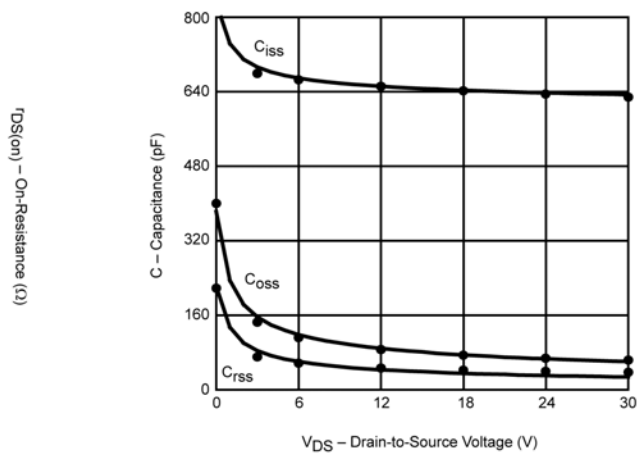
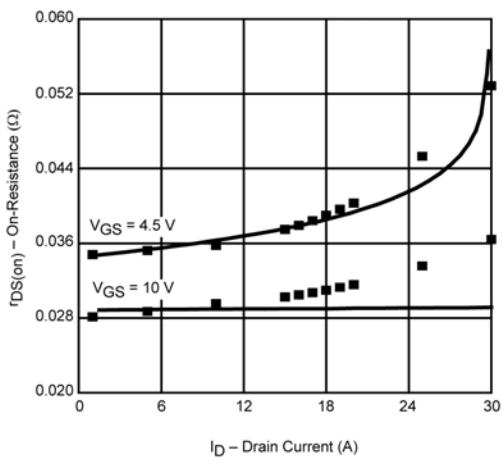
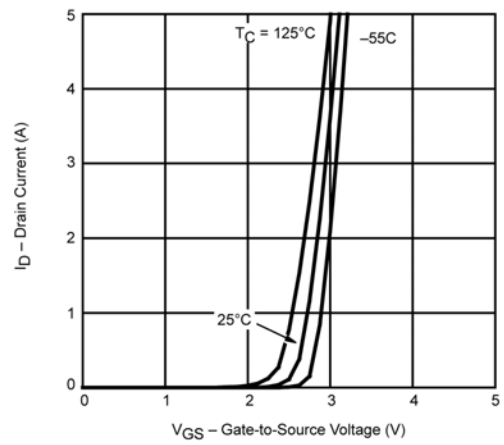
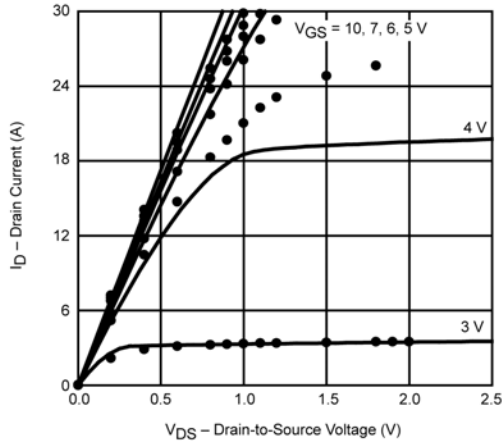
**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ( $T_J=25^\circ\text{C}$  UNLESS OTHERWISE NOTED)

N-Channel MOSFET

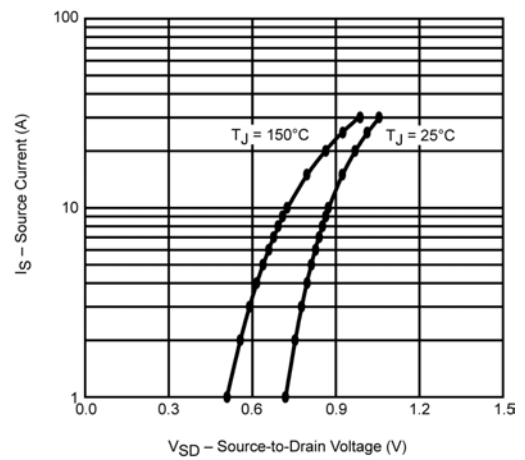
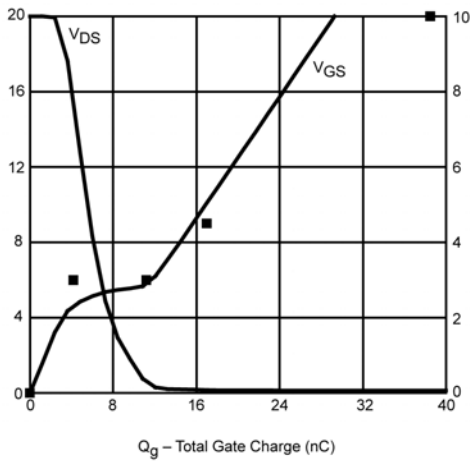
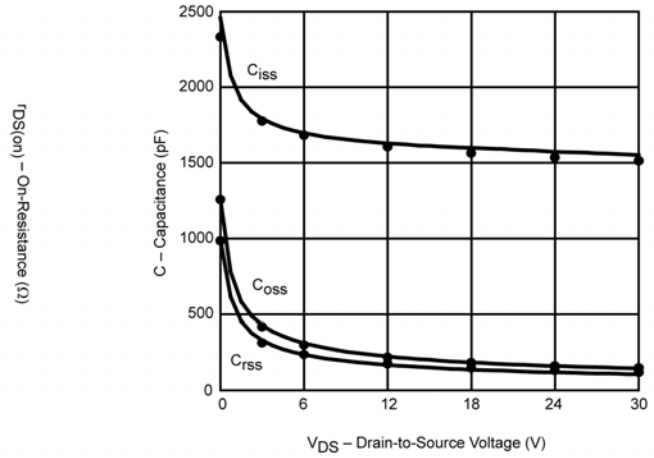
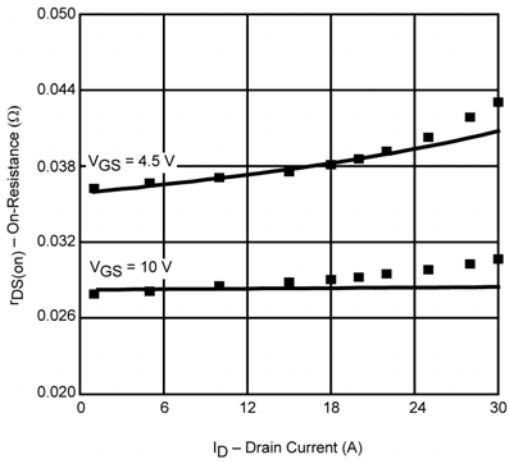
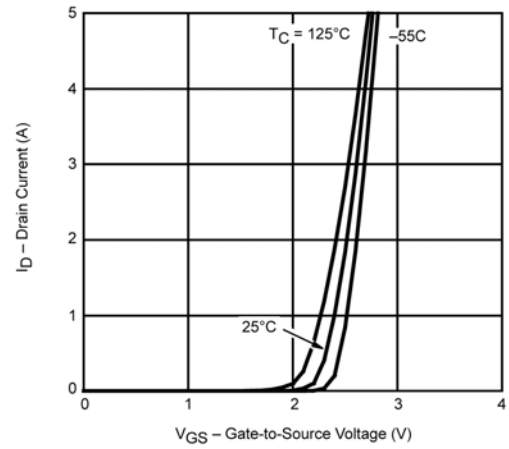
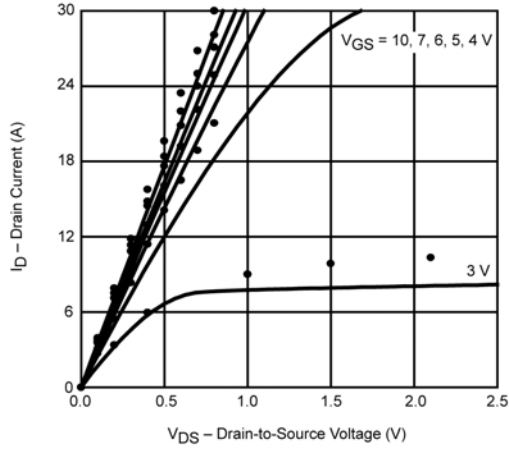


Note: Dots and squares represent measured data.



## Vishay Siliconix

### P-Channel MOSFET



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## Disclaimer

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