Component Video Selector

FEATURES

- Wide Bandwidth: 200 MHz
- Very Low Crosstalk: –70 dB at 5 MHz
- CMOS Compatible
- I^2C Bus Compatible
- Fast Switching—t_{ON}: <200 ns
- Low $r_{DS(on)}$: 44 Ω
- Single Supply Capability

BENEFITS

- Low Insertion Loss
- Improved System Performance
- Reduced Power Consumption
- Easily Interfaced
- Future System Expansion via I^2C Bus

APPLICATIONS

- Component Video Switching: RGB + SYNC, S-VHS, Y-C, etc.
- Audio/Video Routing
- Digital TV
- ATE
- I^2C Bus Audio/Video Systems
- SCART Video Switching

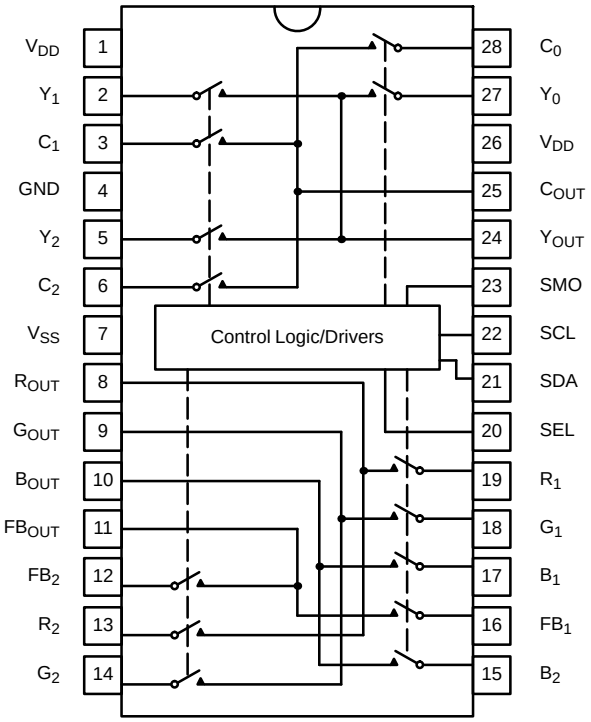
DESCRIPTION

The DG894 is a monolithic video selector designed for switching a variety of component video signals. The low on-resistance and low capacitance of the DG894 make it ideal for video/audio signal routing. Switch control can be through direct CMOS addressing or through the two-wire I^2C bus.

The DG894 is built on the Vishay Siliconix proprietary D/CMOS process that combines n-channel DMOS switching FETs with low-power CMOS control logic and drivers. Low-capacitance DMOS FETs are used to achieve high levels of off isolation at low cost.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

Dual-In-Line and SOIC



Top View

TRUTH TABLE				
SMO	**SEL**	**SDA**	**SCL**	**Function/Switch On**
0	0	I^2C Bus Operation, Address A_0 = "1"		
0	1	I^2C Bus Operation, Address A_0 = "0"		
1	0	0	0	All switches off
1	0	0	1	Y_0, C_0
1	0	1	0	Y_1, C_1
1	0	1	1	Y_2, C_2
1	1	0	0	R_1, G_1, B_1, F_1
1	1	0	1	R_2, G_2, B_2, F_2
1	1	1	0	R_1, G_1, B_1, F_1, Y_1, C_1
1	1	1	1	R_2, G_2, B_2, F_2, Y_2, C_2

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
–40 to 85°C	28-Pin Plastic DIP	DG894DJ
	28-Pin Wide Body SOIC	DG894DW

ABSOLUTE MAXIMUM RATINGS

V+ to GND ..... –0.3 V to 19 V
V+ to V– ..... –0.3 V to 19 V
V– to GND ..... –10 V to 0.3 V
Digital Inputs ..... GND –0.3 V to (V+) +0.3 V
or 20 mA, whichever occurs first
Signal Inputs ..... V_{SS} –0.3 V to 8 V
or 20 mA, whichever occurs first
Continuous Current (Any Terminal) ..... 20 mA
Current (Any Terminal) Pulsed 1 ms, 10% Duty Cycle Max ..... 40 mA
Storage Temperature ..... –65 to 125°C
Power Dissipation (Package)[a]
28-Pin Plastic DIP ..... 625 mW
28-Pin Wide Body SOIC ..... 450 mW

Notes:
a. All leads welded or soldered to PC board.

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} = 12 V, V_{SS} = –5 V V_{INH} = 3 V, V_{INL} = 1.5 V[e]	Temp[a]	Limits –40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}	V_{DD} = 12 V, V_{SS} = GND	Full	0		4	V
		V_{DD} = 12 V, V_{SS} = –5 V	Full	–2		2	
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = –10 mA, V_D = 0 V	Room Full		44 51	100 150	Ω
Resistance Match Between Channels	$\Delta r_{DS(on)}$		Room		10		
Source Off Leakage Current	$I_{S(off)}$	V_S = 4 V, V_D = 0 V	Room Full	–10 –100	–0.05	10 100	nA
Drain Off Leakage Current	$I_{D(off)}$	V_D = 4 V, V_S = 0 V	Room Full	–10 –100	–0.05	10 100	
Total Switch On Leakage Current	$I_{D(on)}$	V_D = V_S = 4 V	Room Full	–10 –100	–0.07	10 100	
Input							
Input Voltage High	V_{INH}		Full	3	2.55		V
Input Voltage Low	V_{INL}		Full		2.55	1.5	
Input Threshold	V_{th}		Room		2.55		
Temp Coefficient of Input Threshold	TC_{th}		Full		–200		µV/°C
Input Current	I_{IN}	V_{IN} = GND or V_{DD}	Room Full	–1 –20	0.05	1 20	µA
Output Voltage Low	V_{OL}	Pin 21, During Acknowledge, I_{OL} = 3 mA	Room			0.4	V
Dynamic							
Input Capacitance[d]	C_{in}	Pin 21, 22	Room		3	10	pF
On State Input Capacitance[d]	$C_{S(on)}$	V_S = V_D = 0 V	Room		10	15	
Off State Input Capacitance[d]	$C_{S(off)}$	V_S = 0 V	Room		4	8	
Off State Output Capacitance[d]	$C_{D(off)}$	V_D = 0 V	Room		4	8	
Bandwidth[d]	BW	R_L = 50 Ω, See Figure 1	Room	200	500		MHz
Turn On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF, 50% to 90% V_{SS} = –5 V, 0 V, V_S = 3 V, See Figure 1	Room			200	ns
Turn Off Time	t_{OFF}		Room			180	
SCL Max Clock Frequency	$F_{SCL(MAX)}$		Full	100			kHz
Component Crosstalk	$X_{TALK(CO)}$	R_{IN} = 10 Ω, R_L = 1 kΩ f = 5 MHz, See Figure 2 and 3	Room		–85		dB
Channel Crosstalk	$X_{TALK(CH)}$		Room		–85		

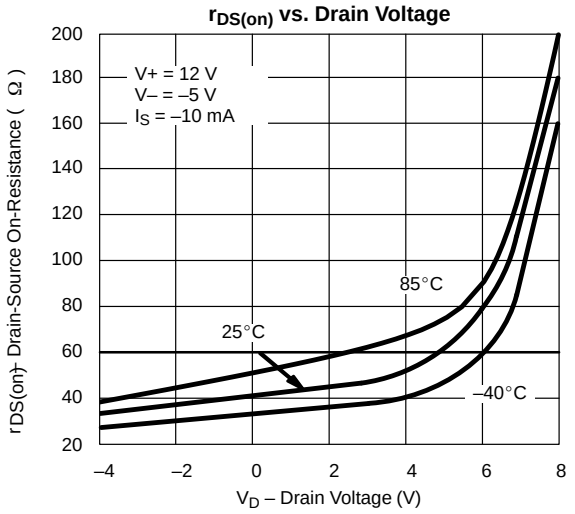
SPECIFICATIONS

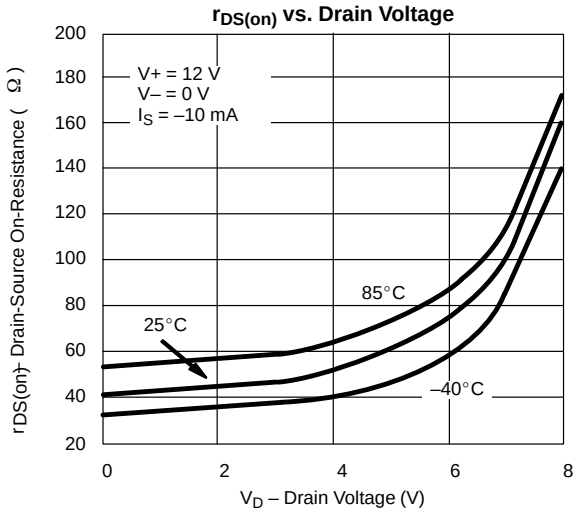
Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} = 12 V, V_{SS} = –5 V, V_{INH} = 3 V, V_{INL} = 1.5 V[e]	Temp[a]	Limits –40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Supply Voltage							
Positive Supply Current	I+	All Control Inputs 0 V, 5 V	Room Full		3 4	8 10	mA
Negative Supply Current	I–		Room Full	–8 –10	–2.5 –3.0		

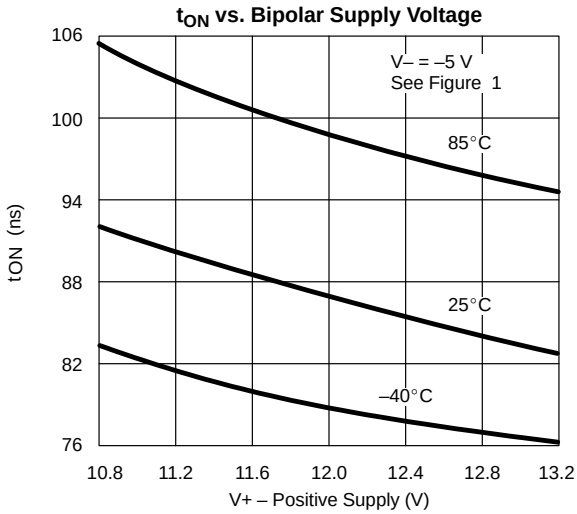
Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

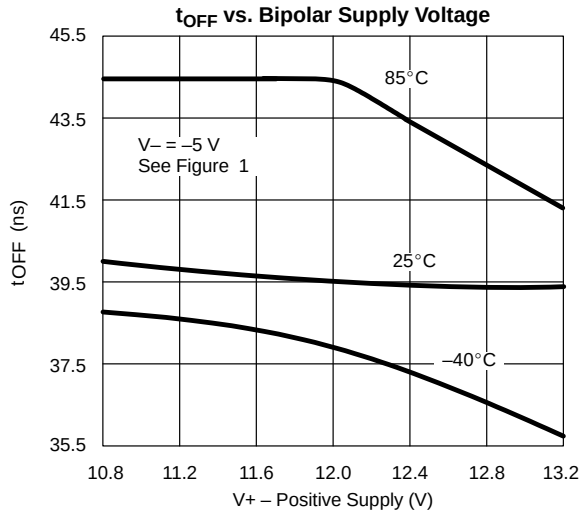
Purchase of Vishay Siliconix DG894 components conveys a license to use them in the I²C system as defined by Philips.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



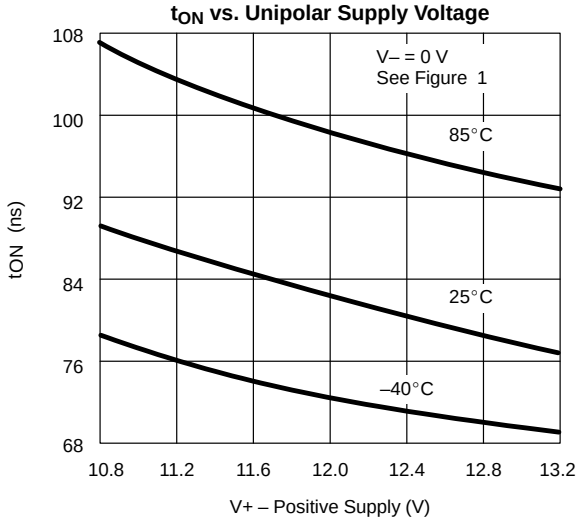




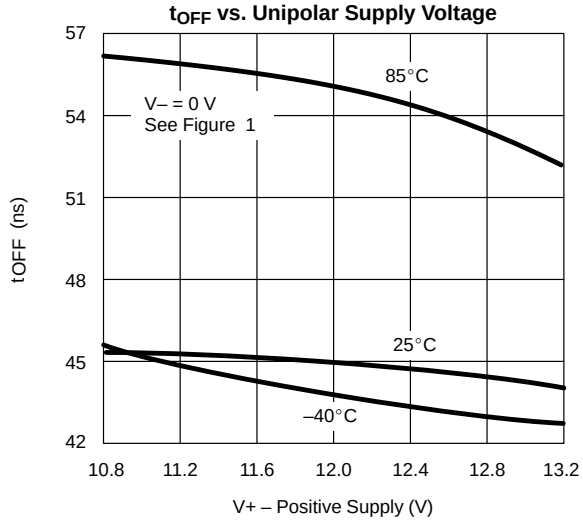


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

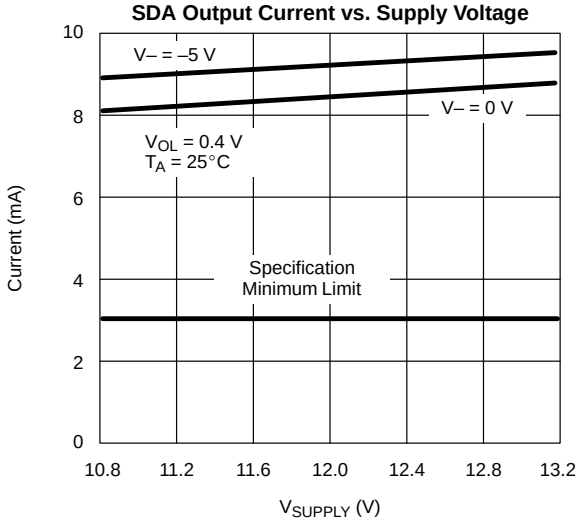
t_{ON} vs. Unipolar Supply Voltage



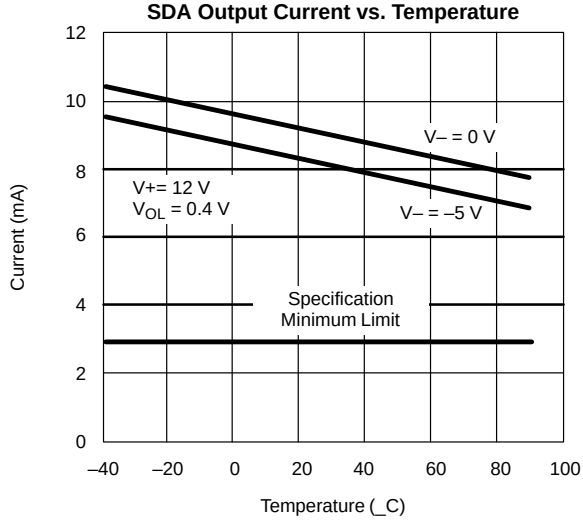
t_{OFF} vs. Unipolar Supply Voltage



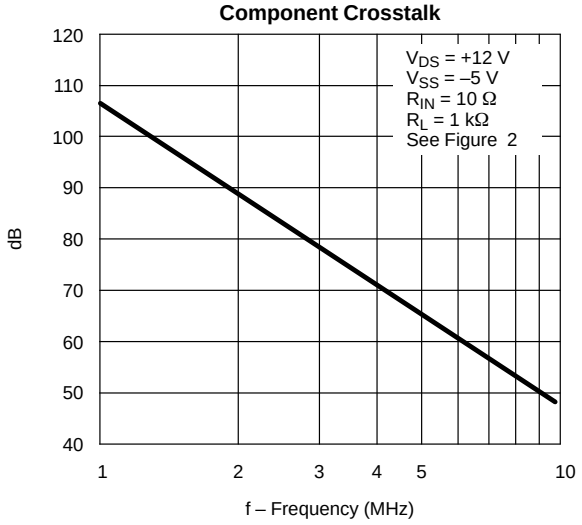
SDA Output Current vs. Supply Voltage



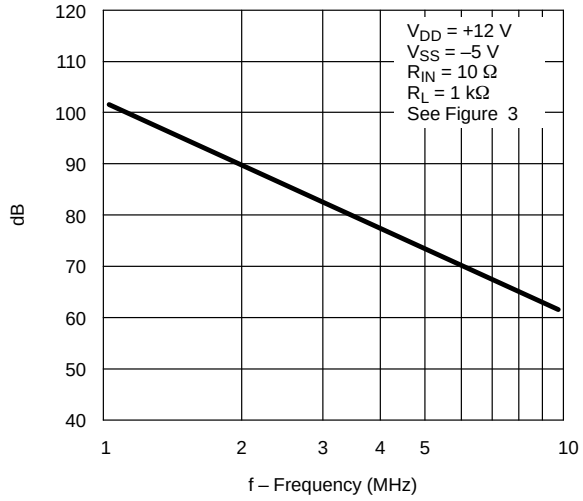
SDA Output Current vs. Temperature



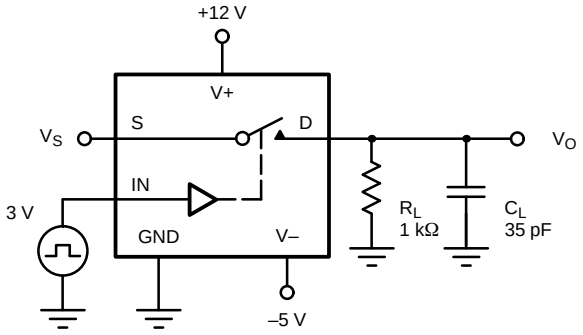
Component Crosstalk

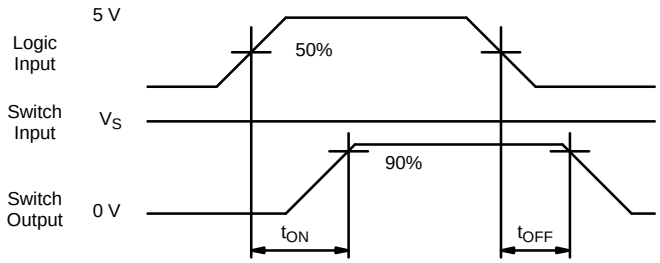


Channel Crosstalk



TEST CIRCUITS

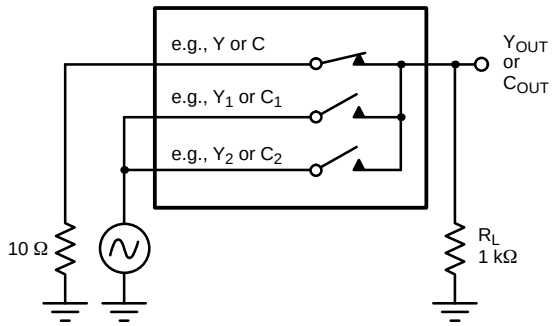




C_L (includes fixture and stray capacitance)

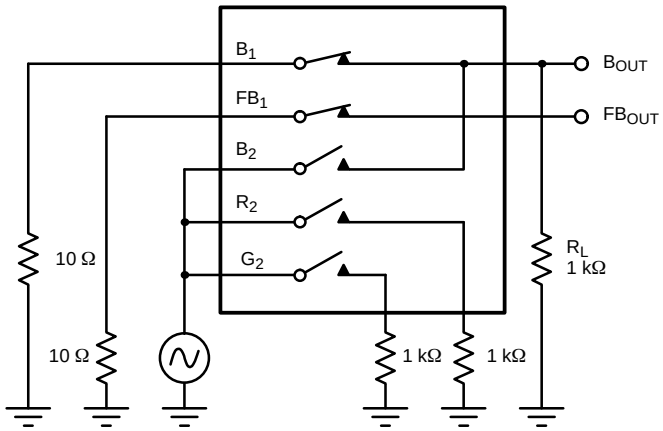
$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

FIGURE 1. Switching Time



$$X_{TALK(CO)} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

FIGURE 2. Component Crosstalk



$$X_{TALK(CH)} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

FIGURE 3. Channel Crosstalk

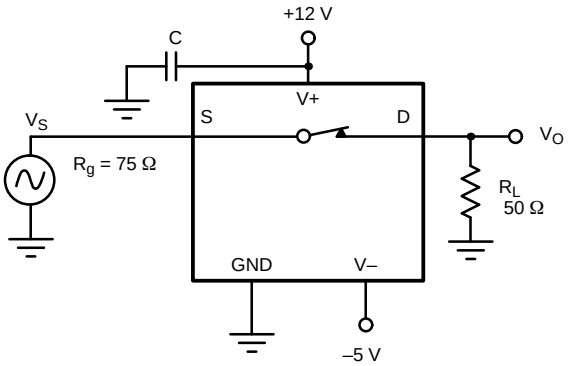


FIGURE 4. Bandwidth

OPERATING VOLTAGE RANGE

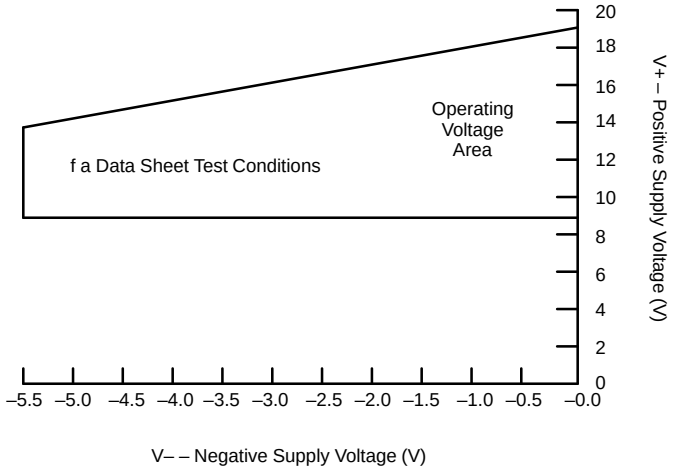


FIGURE 5.

PIN DESCRIPTION

Symbol	Description
Y_0, Y_1, Y_2	An analog channel input, typically luminance.
C_0, C_1, C_2	An analog channel input, typically chrominance.
R_1, R_2, G_1, G_2, B_1, B_2, FB_1, FB_2	An analog channel input, typically “red”, “green”, “blue” or “fast blanking”, as appropriate.
GND	Analog and digital ground.
V_{DD}	Positive supply voltage[a]
V_{SS}	Negative supply voltage
Y_{OUT}, C_{OUT}	An analog channel output, typically luminance or chrominance, as appropriate
R_{OUT}, G_{OUT}, B_{OUT}, FB_{OUT}	An analog channel output, typically “red”, “green”, “blue” or “fast blanking”, as appropriate.
SMO	A low selects serial mode (I^2C) operation. A high selects CMOS operation.
SDA	Serial data line[b]
SCL	Serial clock line[b]
SEL	CMOS control line or I^2C address[c] select line

Notes:
a. Both V_{DD} pins (Pin 1 and Pin 26) must be connected for proper operation.
b. SDA and SCL pins become CMOS control inputs when SMO = High.
c. The SEL pin, in I^2C bus operation (i.e., with SMO low), is the least significant bit of the device address. This allows two devices to operate on the same I^2C bus, yet retain independent control.

APPLICATIONS

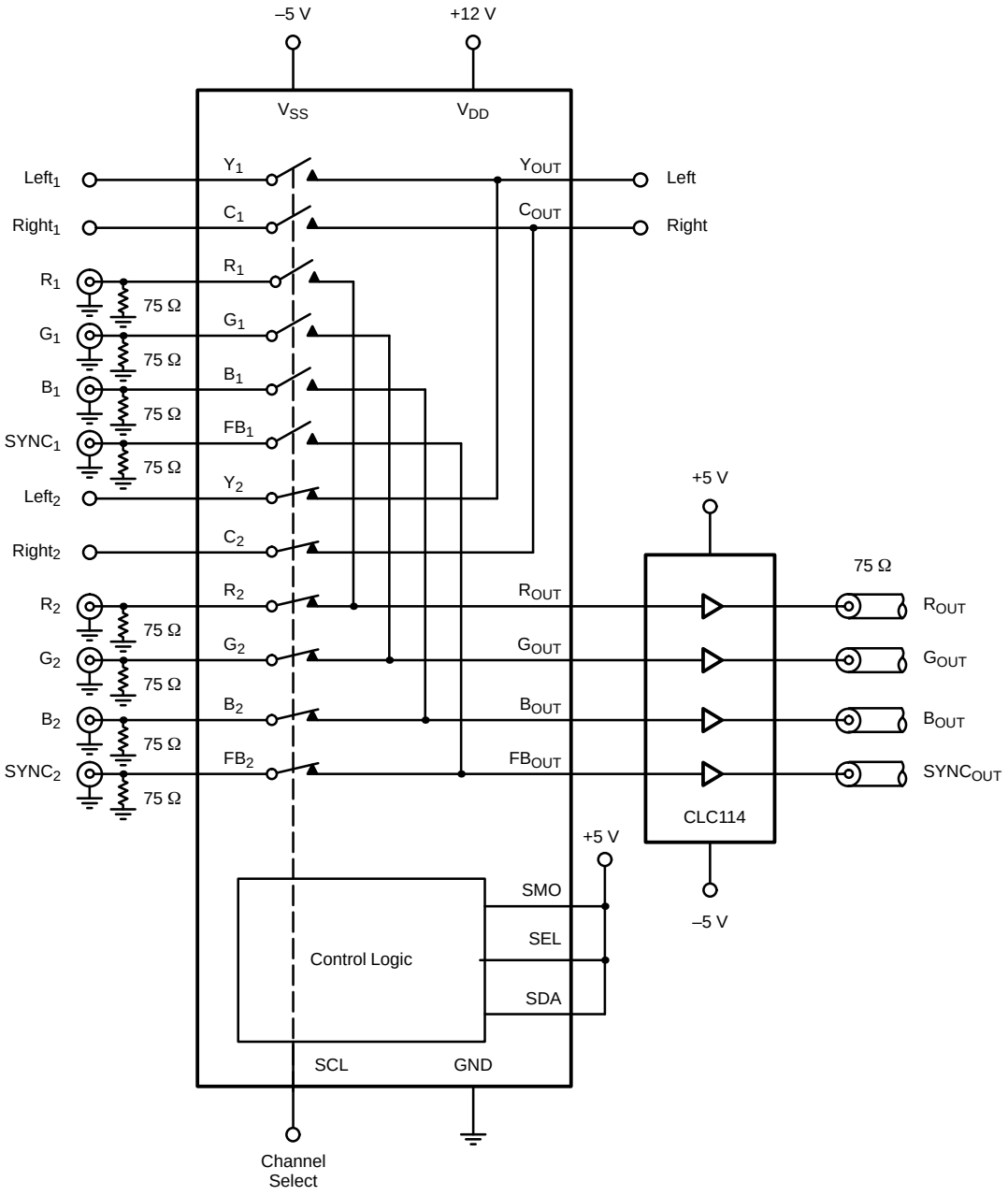


FIGURE 6.

I²C Bus Operation—RGB Switching

Figure 6 shows an inexpensive RGB + stereo selector. The two audio channels are switched via the C, Y terminals. The CLC114 quad video buffer drives four 75-Ω output lines.

Characteristics of the I²C Bus

The I²C Bus interface is ideally suited for communication between different ICs or modules. Its salient features are:

- Two wire bidirectional serial bus
  - Serial data (SDA) and serial clock (SCL) lines
- Multi-master system (built-in arbitration for multi-master systems)
- Devices have independent clocks
- Master and slave devices can be receivers and/or transmitters.
- Each device has a unique address.
- Maximum bus clock rate of 100 kHz.
- Any number of interfaces may be connected to the bus
  - Limited only by total capacitance of 400 pF
  - Each pin on bus limited to 10-pF capacitance
  - Input levels:
    V_{IL} max = 1.5 V (fixed supply operation)
    V_{IH} min = 3 V (fixed supply operation)
    V_{IL} max = 0.3 V_{DD} (wide range supply operation)
    V_{IH} min = 0.7 V_{DD} (wide range supply operation)

System Configuration

R_p value depends on:

- number of devices on bus
- total bus capacitance
- supply voltage (Figure 7).

Data Transfer on the I²C Bus

If the bus is not being used, both SDA and SCL lines must be left high.

Every byte put onto the SDA line should be eight bits long (MSB first), followed by an acknowledge bit, which is generated by the receiving device.

Each data transfer is initiated with a start condition and ended with a stop condition. The first byte after a start condition is always the address byte. If this is the device's own address, the device will generate an acknowledge by pulling the SDA line low during the ninth clock pulse, then accept the data in subsequent bytes until another start or stop condition is detected.

The eight bit of the address byte is the read/write bit (high = read from addressed device, low = write to the addressed device) so, for the DG894, the address is only considered valid if the R/W bit is low.

Data bytes are always acknowledged during the ninth clock pulse by the addressed device. Note that during the acknowledge period the transmitting device must leave the SDA line high.

Premature termination of the data transfer is allowed by generating a stop condition at any time. When this happens, the DG894 will remain in the state defined by the last complete data byte transmitted.

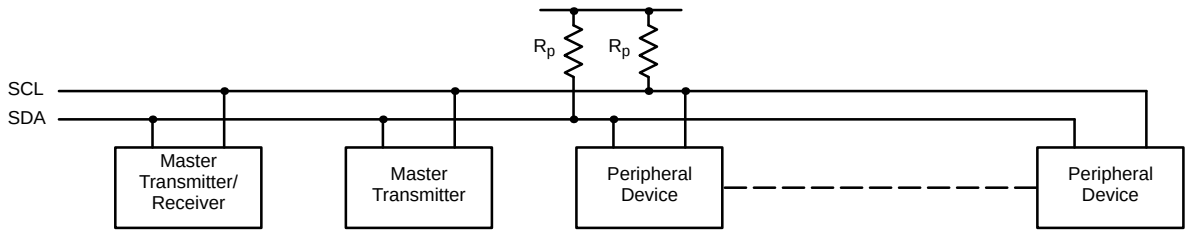


FIGURE 7.

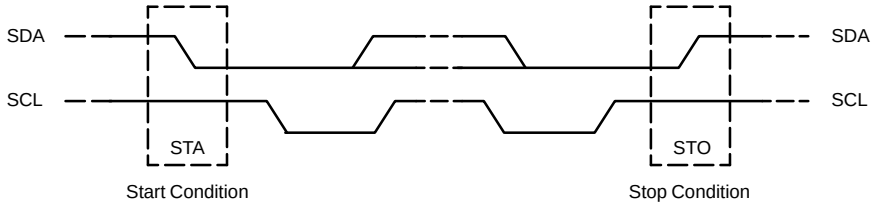


FIGURE 8. START and STOP Conditions

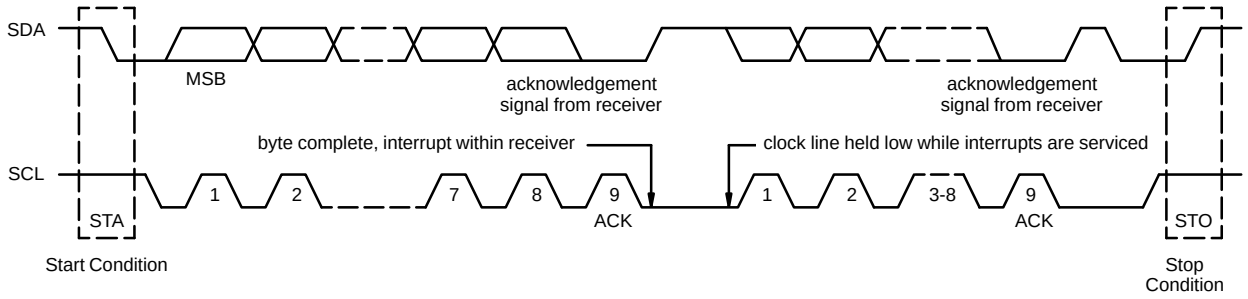


FIGURE 9. Data Transfer on the I^2C Bus

Timing Specifications of the I^2C Bus

I^2C bus load conditions for timing specifications are as follows:

4 kΩ pull-up resistors to +5 V; 200 pF capacitor to ground. All values are referred to V_{IH} = 3 V, V_{IL} = 1.5 V.

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	–	100	kHz
Bus Free Before Start	t_{BUF}	4.7	–	µs
Start Condition Set-up Time	$t_{SU;STA}$	4.7	–	
Start Condition Hold Time	$t_{HD;STA}$	4	–	
SCL and SDA Low Period	t_{LOW}	4.7	–	
SCL and SDA High Period	t_{HIGH}	4	–	
SCL and SDA Rise Time	t_r	–	1.0	
SCL and SDA Fall Time	t_f	–	0.3	
Data Set-Up Time (WRITE)	$t_{SU;DAT}$	0.25	–	
Data Hold Time (WRITE)	$t_{HD;DAT}$	0*	–	

*A transmitter must internally provide at lease a hold time to bridge the undefined region (max 300 ns) of the falling edge of the SCL.

I^2C Bus Protocol

The DG894 is a slave receiver type of I^2C interface and has four allocated addresses, two of which are user programmable through the SEL pin. Additional addresses may be obtained by a metal mask option for users requiring more than two DG894s on the same I^2C bus. Contact Vishay Siliconix marketing for further information.

After the correct address has been sent, only one data byte is needed to define the switch configuration. Subsequent data put onto the bus will update the switches until a STOP condition (or another START condition) signals that the device is no longer being addressed. The switches will then remain in their last configuration as long as power is maintained to the chip.

Power on Reset

A power on reset function is provided on the DG894 to turn all switches off following power up if the I^2C mode is selected. In the CMOS control mode, the switches are selected according to the state of the control inputs.

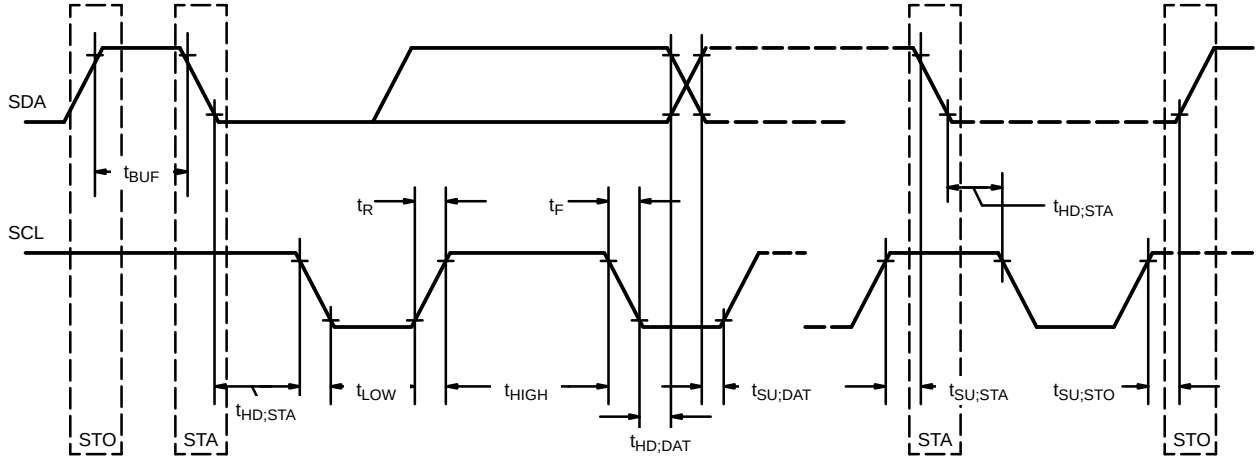


FIGURE 10. I^2C Bus Timing Diagram

Minimum Bit Stream to Set Up DG894 Switches

STA	1	1	0	1	1	A_1	A_0	R/W	ACK	X	X	X	D_4	D_3	D_2	D_1	D_0	ACK	STO

Address Byte — Data Byte

STA = START CONDITION
A_1 = 0 (programmable to “1” with metal mask change)
A_0 = $\overline{SEL}$. Address bit set by use (address is inverse of SEL logic level)
R/W = READ/WRITE bit (must be “0”, only WRITE mode allowed for DG894)
ACK = Acknowledge bit (“0”) generated by DG894
D_4 = 0 — R_2, G_2, B_2, and FB_2 switches off
D_4 = 1 — R_2, G_2, B_2, and FB_2 switches on
D_3 = 0 — R_1, G_1, B_1, and FB_1 switches off
D_3 = 1 — R_1, G_1, B_1, and FB_1 switches on
D_2 = 0 — Y_2, C_2, switches off
D_2 = 1 — Y_2, C_2, switches on
D_1 = 0 — Y_1, C_1, switches off
D_1 = 1 — Y_1, C_1, switches on
D_0 = 0 — Y_0 and C_0 switches off
D_0 = 1 — Y_0 and C_0 switches on
STO = STOP CONDITION

Disclaimer

All product specifications and data are subject to change without notice.

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