

# SPICE Device Model Si4308DY

## **Vishay Siliconix**

# Dual N-Channel 30-V (D-S) MOSFET with Schottky Diode

### **CHARACTERISTICS**

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

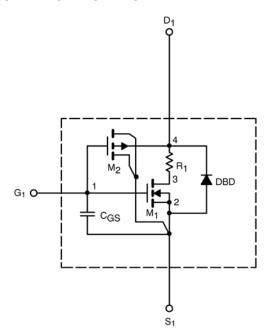
- Apply for both Linear and Switching Application
- Accurate over the –55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

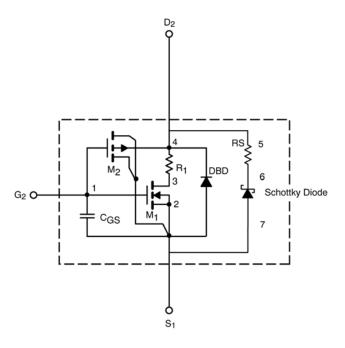
### **DESCRIPTION**

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{\rm gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### SUBCIRCUIT MODEL SCHEMATIC





This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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Parameter	Symbol	Test Conditions		Simulated Data	Measured Data	Unit
Static	<u> </u>			<u>!</u>		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}$ = $V_{GS}$ , $I_D$ = 250 $\mu A$	Ch-1	1.25	1.4	V
			Ch-2	0.95	1.35	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	Ch-1	398		А
			Ch-2	622		
Drain-Source On-State Resistance <sup>a</sup>	Γ <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, I_D = 9.6 \text{ A}$	Ch-1	0.010	0.010	Ω
		$V_{GS}$ = 10 V, $I_D$ = 13.5 A	Ch-2	0.0078	0.0070	
		$V_{GS} = 4.5 \text{ V}, I_D = 7.8 \text{ A}$	Ch-1	0.015	0.015	
		$V_{GS}$ = 4.5 V, $I_{D}$ = 12.5 A	Ch-2	.0092	0.0085	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 9.6 A	Ch-1	31	25	S
		$V_{DS}$ = 15 V, $I_{D}$ = 13.5 A	Ch-2	51	56	
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	$I_{S} = 1.8 \text{ A}, V_{GS} = 0 \text{ V}$	Ch-1	0.70	0.70	V
		I <sub>S</sub> = 2.7 A, V <sub>GS</sub> = 0 V	Ch-2	0.470	0.485	
Dynamic <sup>b</sup>						
Total Gate Charge	$Q_g$		Ch-1	11	11.5	
		Channel-1	Ch-2	35	40	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 15 \text{ V}, V_{GS} = 5 \text{ V}, I_{D} = 9.6 \text{ A}$	, = 9.6 A Ch-1 3 3	3	nC	
		Channel-2 $V_{DS} = 15 \text{ V}, V_{GS} = 5 \text{ V}, I_D = 13.5 \text{ A}$	Ch-2	10	10	iic
Gate-Drain Charge	$Q_{gd}$		Ch-1	4.5	4.5	
			Ch-2	8.8	8.8	
Turn-On Delay Time	t <sub>d(on)</sub>		Ch-1	10	10	ns
		$Channel-1 \\ V_{DD} = 15 \text{ V, } R_L = 15 \Omega \\ I_D \cong 1 \text{ A, } V_{GEN} = 10 \text{ V, } R_G = 6 \Omega \\ Channel-2 \\ V_{DD} = 15 \text{ V, } R_L = 15 \Omega \\ I_D \cong 1 \text{ A, } V_{GEN} = 10 \text{ V, } R_G = 6 \Omega \\ \label{eq:DD}$	Ch-2	19	17	
Turn-Off Delay Time	$t_{d(off)}$		Ch-1	15	5	
			Ch-2	23	14	
			Ch-1	22	30	
Fall Time	t <sub>f</sub>		Ch-2	48	102	
			Ch-1	40	10	
			Ch-2	61	26	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	$I_F = 1.8 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$	Ch-1	30	30	
		I <sub>F</sub> = 2.7 A, di/dt = 100 A/μs	Ch-2	37	40	

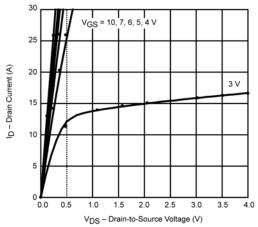
a. Guaranteed by design, not subject to production testing. b. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2%.

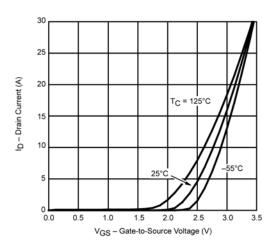


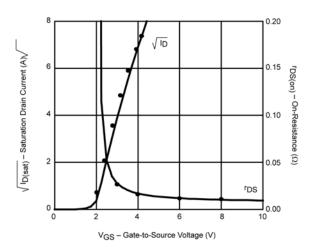
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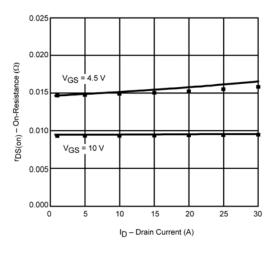
### COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)

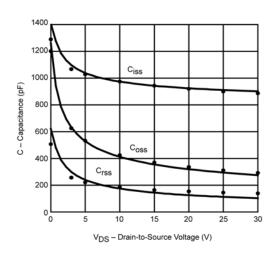
### Channel 1

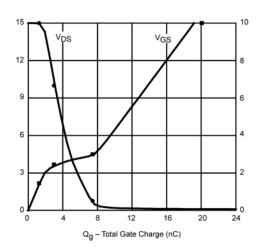












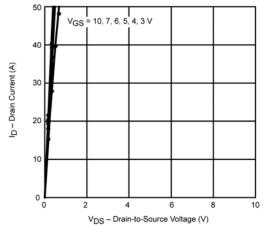
Note: Dots and squares represent measured data.

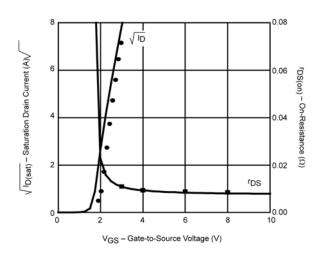
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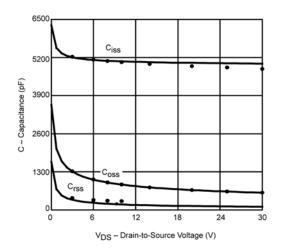
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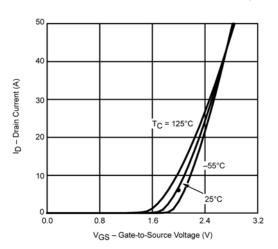
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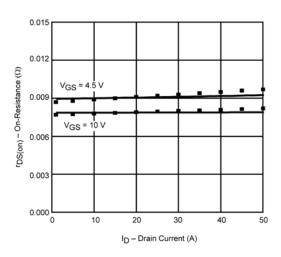


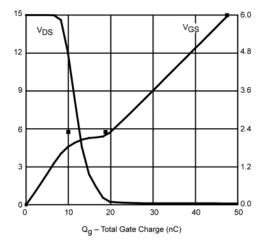












Note: Dots and squares represent measured data.



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