



Dual N-Channel 30-V (D-S) MOSFET with Schottky Diode

CHARACTERISTICS

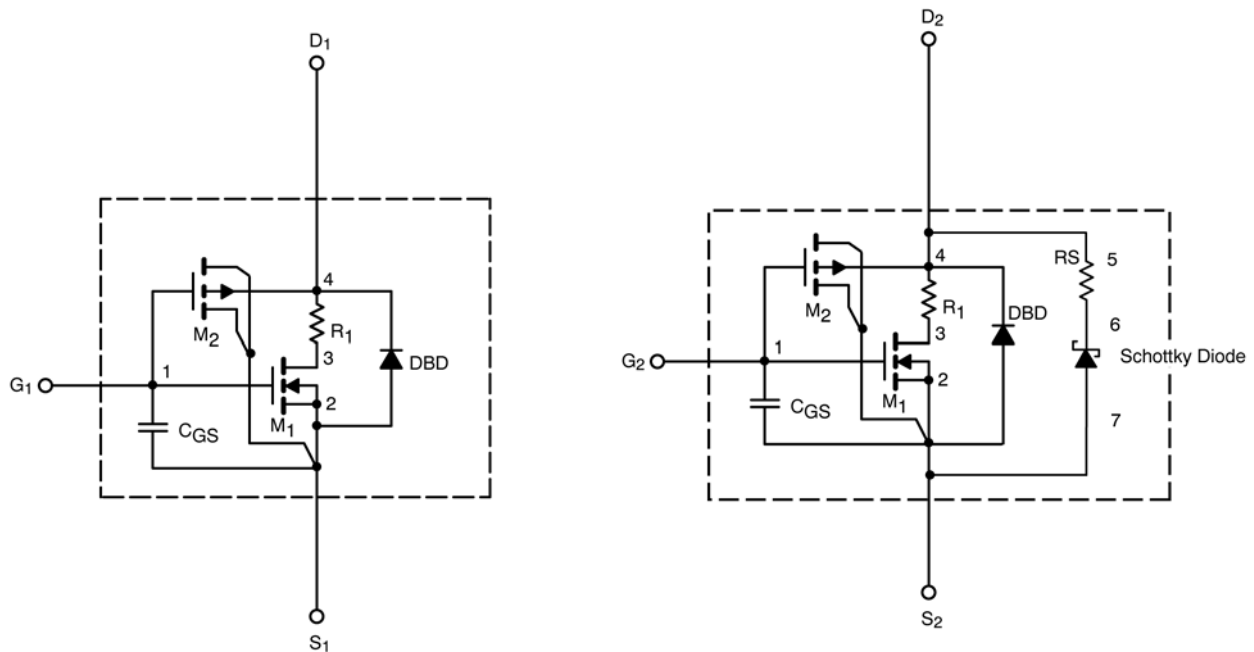
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition		Simulated Data	Measured Data	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	Ch-1	1.25	1.4	V
			Ch-2	0.95	1.35	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	Ch-1	398		A
			Ch-2	622		
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 9.6 A	Ch-1	0.010	0.010	Ω
		V _{GS} = 10 V, I _D = 13.5 A	Ch-2	0.0078	0.0070	
		V _{GS} = 4.5 V, I _D = 7.8 A	Ch-1	0.015	0.015	
		V _{GS} = 4.5 V, I _D = 12.5 A	Ch-2	.0092	0.0085	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 9.6 A	Ch-1	31	25	S
		V _{DS} = 15 V, I _D = 13.5 A	Ch-2	51	56	
Diode Forward Voltage ^a	V _{SD}	I _S = 1.8 A, V _{GS} = 0 V	Ch-1	0.70	0.70	V
		I _S = 2.7 A, V _{GS} = 0 V	Ch-2	0.470	0.485	
Dynamic^b						
Total Gate Charge	Q _g	Channel-1 V _{DS} = 15 V, V _{GS} = 5 V, I _D = 9.6 A Channel-2 V _{DS} = 15 V, V _{GS} = 5 V, I _D = 13.5 A	Ch-1	11	11.5	nC
Gate-Source Charge	Q _{gs}		Ch-2	35	40	
			Ch-1	3	3	
Gate-Drain Charge	Q _{gd}		Ch-2	10	10	
			Ch-1	4.5	4.5	
			Ch-2	8.8	8.8	
		Ch-1	10	10		
Turn-On Delay Time	t _{d(on)}	Channel-1 V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω Channel-2 V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω	Ch-2	19	17	ns
Turn-Off Delay Time	t _{d(off)}		Ch-1	15	5	
			Ch-2	23	14	
			Ch-1	22	30	
			Ch-2	48	102	
Fall Time	t _f		Ch-1	40	10	
			Ch-2	61	26	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = 1.8 A, di/dt = 100 A/μs	Ch-1	30	
		I _F = 2.7 A, di/dt = 100 A/μs	Ch-2	37	40	

Notes

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

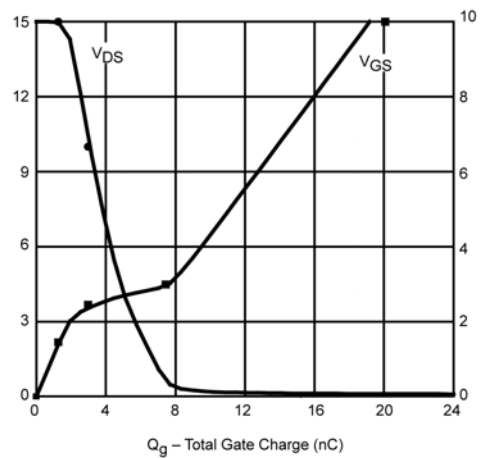
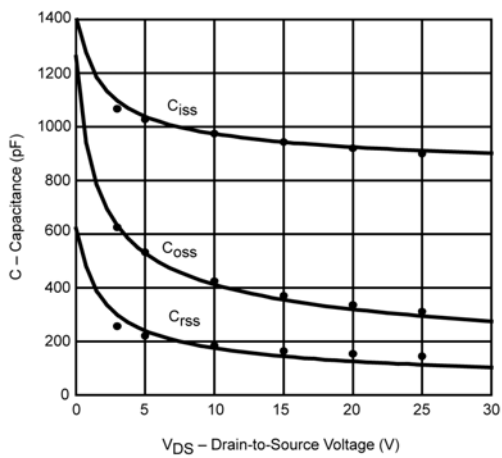
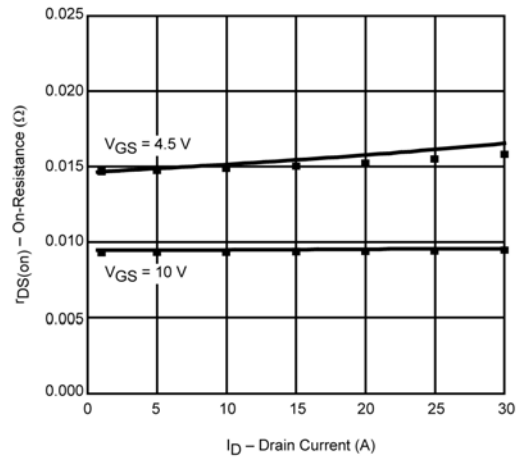
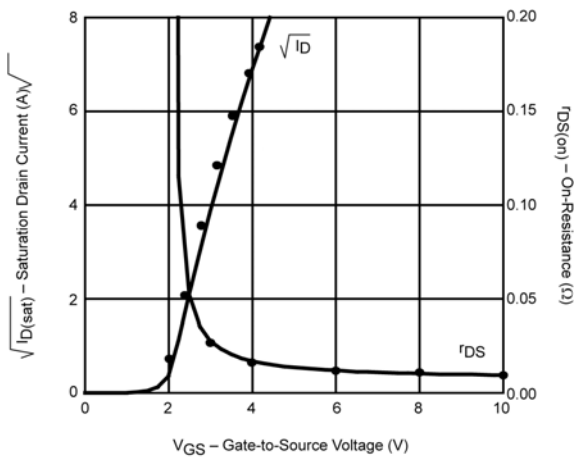
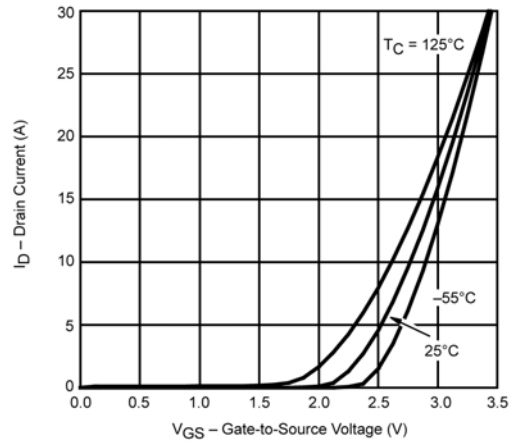
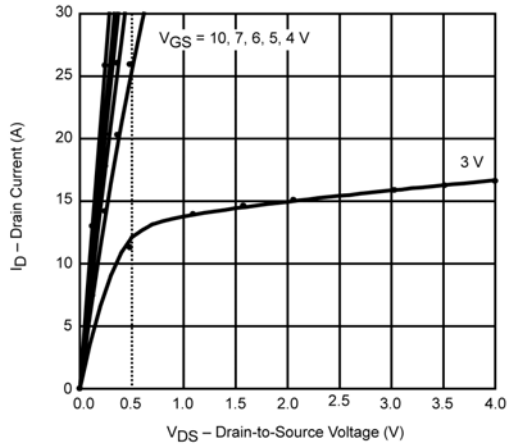


SPICE Device Model Si4310DY

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COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Channel 1

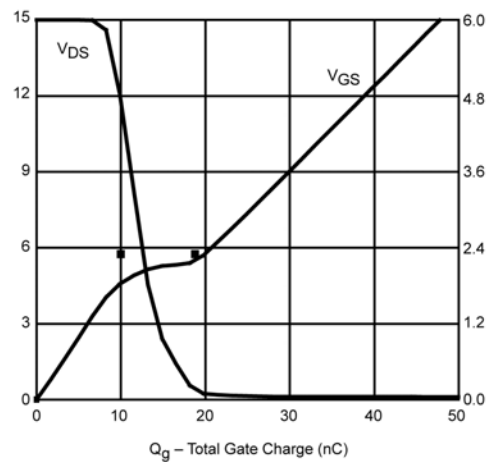
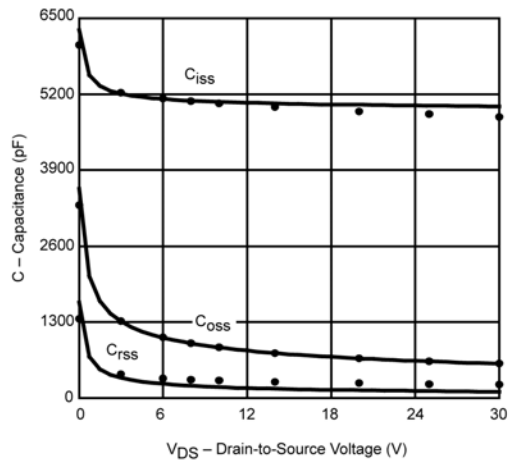
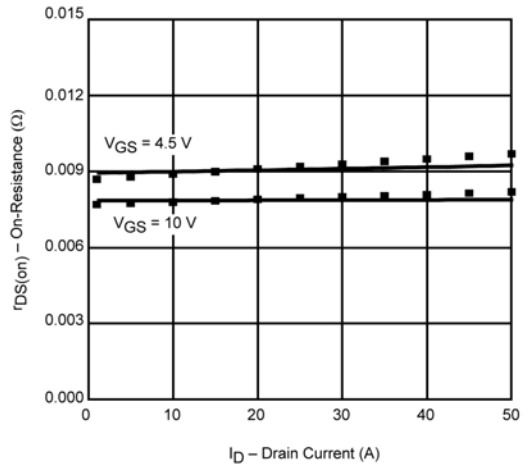
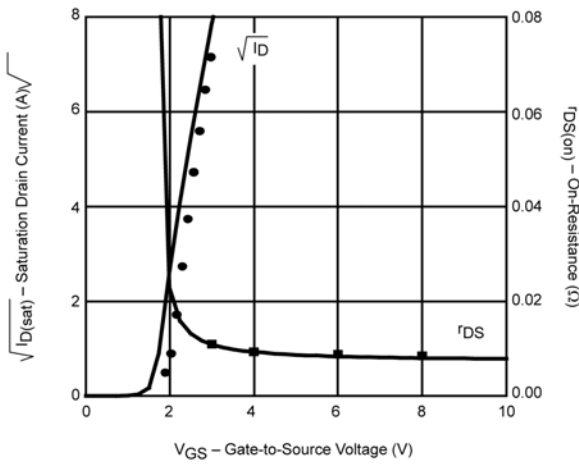
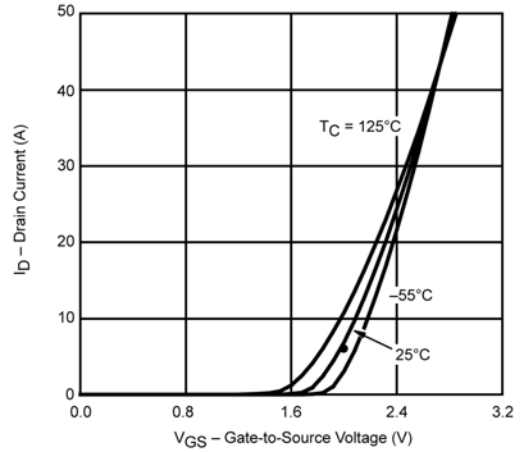
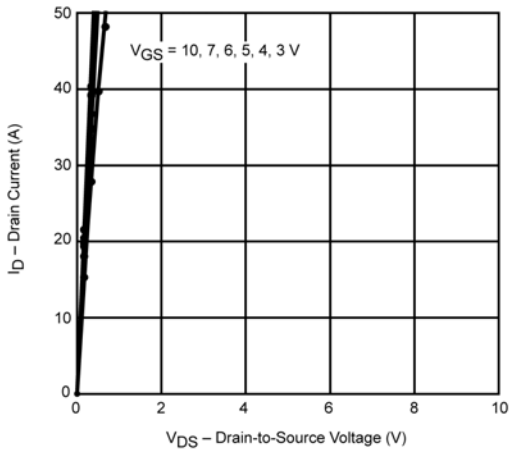


Note: Dots and squares represent measured data.



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Channel 2



Note: Dots and squares represent measured data.



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