

# Synchronous Buck Controller for High Performance Processors

## FEATURES

- Over-Voltage Protection
- Programmable Over-Current Protection
- Voltage Mode Control
- Precision 1.3-V,  $\pm 1.6\%$  Reference
- Drives N-Channel Switch and Rectifier
- 800- $\mu$ A Quiescent Current ( $f_s = 200$  kHz)
- 150- $\mu$ A Standby Current
- Integrated "Power Good" Output
- Synchronization
- Under-Voltage Lockout

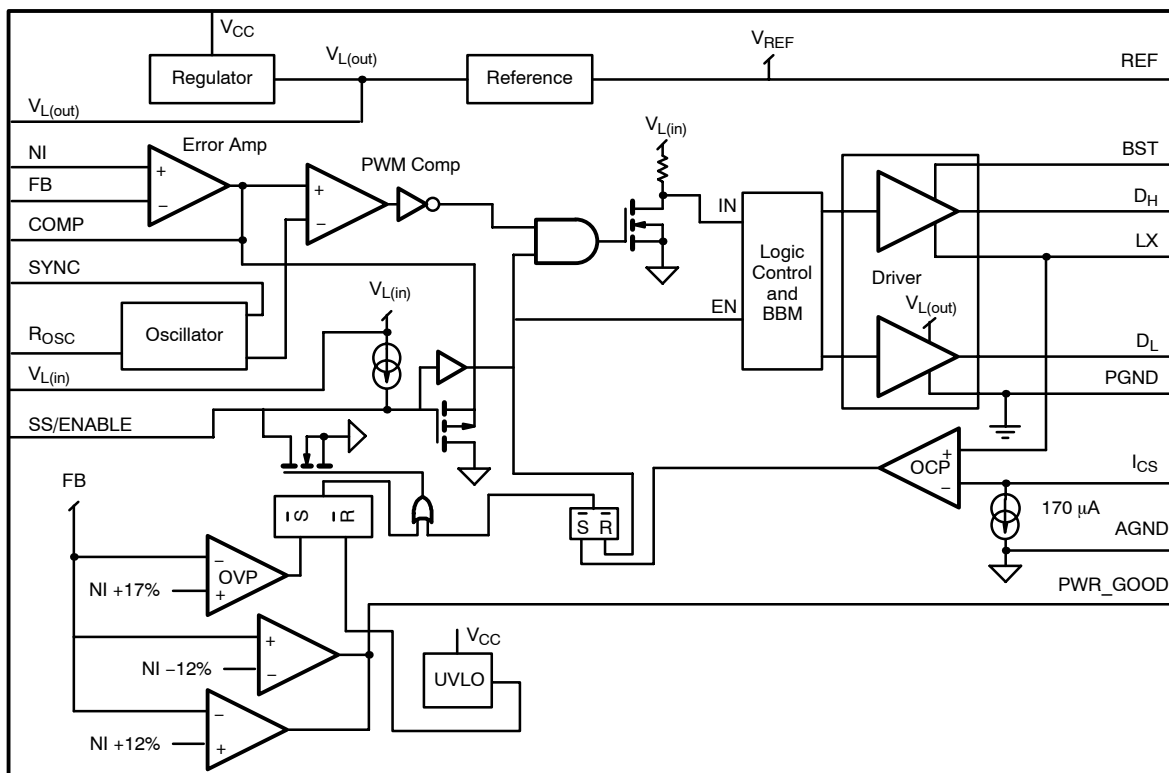
## DESCRIPTION

The voltage mode, synchronous buck controller is designed for point-of-use dc/dc conversion in high performance server and desktop computers. High efficiency is accomplished at full load by driving high- and low-side n-channel MOSFETs. The input voltage range has been designed for 4.75 V to 13.2 V to allow use of either 5 V or 12 V. The 1-MHz switching frequency combined with the 10-MHz error amplifier provides ultra-fast transient response necessary in a high performance microprocessor power supply.

Si9142 is available in both standard and lead (Pb)-free 20-pin SOIC wide-body packages and specified to operate over the commercial ( $0^\circ$  to  $70^\circ\text{C}$ ) temperature range.

A demo board, Si9142DB, is available.

## FUNCTIONAL BLOCK DIAGRAM





## ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to AGND

$V_{\text{SYNC\_IN}}$  ..... -0.3 to 7 V

$V_{\text{SYNC\_OUT}}$  ..... -0.3 to 7 V

$V_{\text{CC}}$  ..... -0.3 to 15 V

Voltages Referenced to PGND

$V_{\text{BST}}$  ..... -0.3 to 20 V

$V_{\text{PGND}}$  to  $V_{\text{AGND}}$  .....  $\pm 2$  V

$V_{\text{L}}$  Short to GND ..... Continuous

$V_{\text{REF(OUT)}}$  Short to GND ..... Continuous

Continuous Power Dissipation ( $T_A = 25^\circ\text{C}$ )<sup>a</sup>

20-Pin SOIC Wide-Body<sup>b</sup> ..... 1.45 W

Operating Temperature Range ..... 0 to 70°C

Storage Temperature Range ..... -65 to 125°C

Lead Temperature (soldering, 10 sec) ..... 300°C

$T_{\text{JMAX}}$  ..... 150°C

$\Theta_{\text{JA}}$  ..... 86°C/W

### Notes

a. Device mounted with all leads soldered or welded to PC board.

b. Derate 11.6 mW/°C above 25°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

$V_{\text{CC}}$  ..... 4.75 V to 13.2 V

$R_{\text{OSC}}$  ..... 100 k $\Omega$  (100 kHz) to 10 k $\Omega$  (1 MHz)

$V_{\text{L(out), (in)}}$  Capacitance ..... 4.7  $\mu\text{F}$

$V_{\text{L(out)}}$  Load .....  $\leq 1$  mA

$V_{\text{REF}}$  Capacitance ..... 0.1  $\mu\text{F}$

$V_{\text{REF}}$  Load .....  $\leq 1$  mA

Analog and Digital Inputs ..... 0 to  $V_{\text{L}}$

SPECIFICATIONS						
Parameter	Specific Test Conditions $V_{\text{CC}} = 4.75$ V to 13.2 V		Limits $T_A = 0$ to 70°C			Unit
			Min <sup>a</sup>	Typ <sup>b</sup>	Max <sup>a</sup>	
<b>Reference</b>						
Output Voltage	$I_{\text{REF}} = 0$		1.30 -1.6%	1.30	1.30 +1.6%	V
Regulation	$I_{\text{REF}} = 0$ to 1 mA		-10		10	mV
Line Rejection	At 10 kHz			80		dB
<b>Oscillator</b>						
Operating Frequency	Sync = Open		100		1000	kHz
PWM Maximum Duty Cycle	$f_{\text{OSC}} = 200$ kHz			94		%
	$f_{\text{OSC}} = 400$ kHz			88		
SYNC High	$I_{\text{OH}} = -100$ $\mu\text{A}$			$0.7 V_{\text{L}}$		V
SYNC Low	$I_{\text{OL}} = 500$ $\mu\text{A}$			$0.3 V_{\text{L}}$		
<b>Output Drivers</b>						
Source/Sink I (Peak)	$\text{BST} - \text{LX} = 4.5$ V	H Driver	500	1000		mA
	$V_{\text{CC}} = 4.75$ V	L Driver	500	1000		
<b>Supply</b>						
Quiescent Current PWM	$f_{\text{OSC}} = 200$ kHz			800	1200	$\mu\text{A}$
Standby Current Shutdown	$V_{\text{CC}} < 3.5$ V			150	225	
<b><math>V_{\text{L}}</math></b>						
Output Voltage	$I_{\text{VL}} = 0, V_{\text{CC}} = 5.7$ to 13.2 V		4.95	5.7	6.05	V
	$I_{\text{VL}} = 0, V_{\text{CC}} = 4.7$ to 5.7 V			$V_{\text{IN}} - 0.2$ V		
Line Rejection	At 10 kHz			30		dB

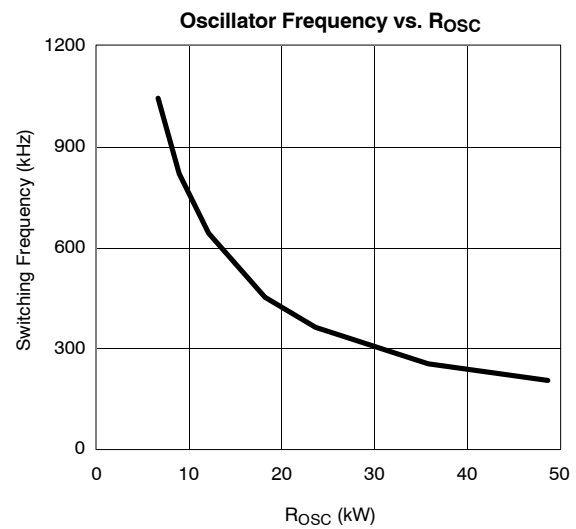
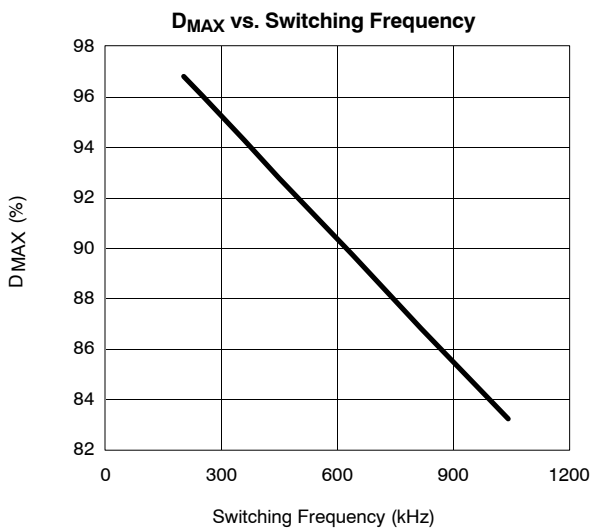
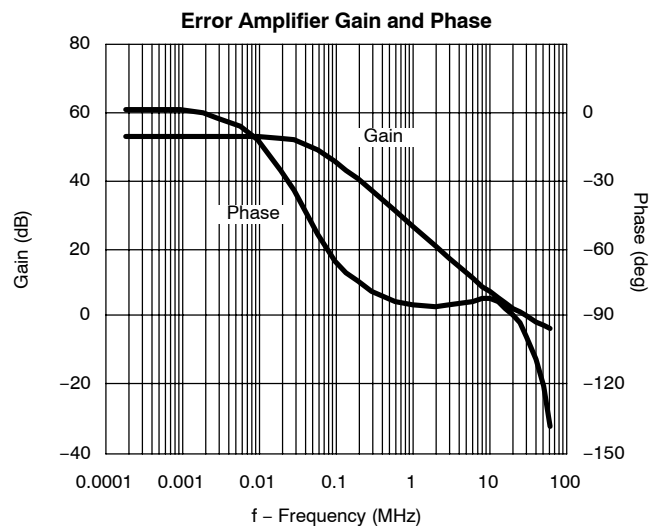
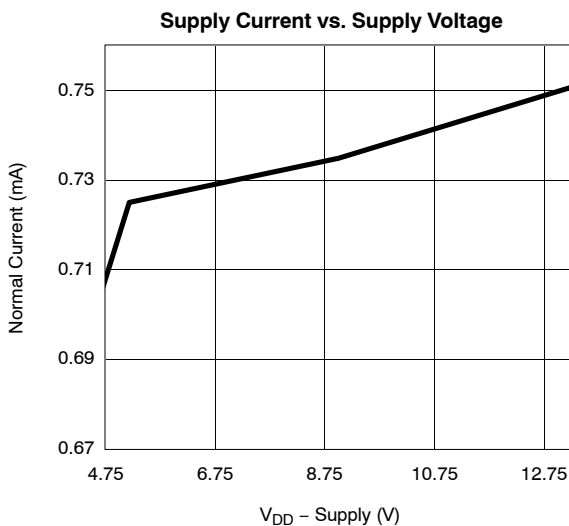
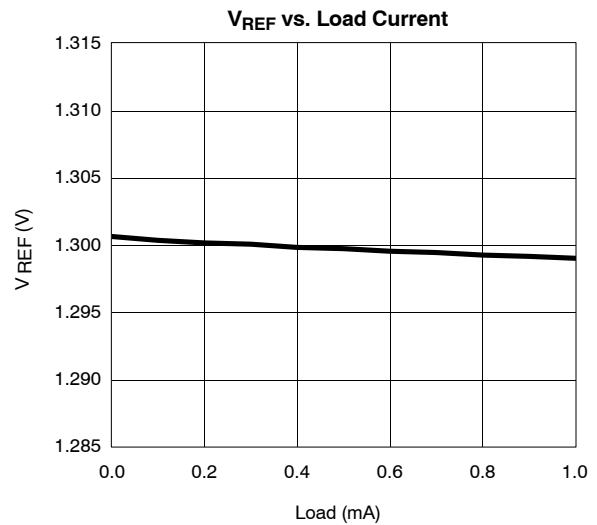
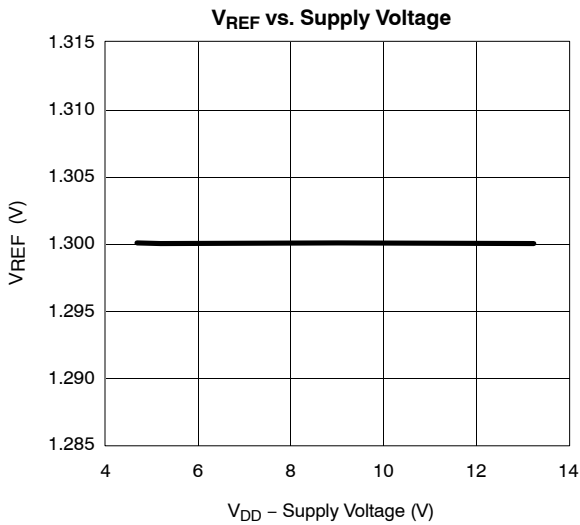


SPECIFICATIONS					
Parameter	Specific Test Conditions $V_{CC} = 4.75 \text{ V to } 13.2 \text{ V}$	Limits $T_A = 0 \text{ to } 70^\circ\text{C}$			Unit
		Min <sup>a</sup>	Typ <sup>b</sup>	Max <sup>a</sup>	
<b>SS/Enable</b>					
Source Current		-2.5	-5	-7.5	$\mu\text{A}$
Fault Sink Current		20	35		mA
Logic Low				0.8	V
Logic High		2.4			
<b>UVLO</b>					
Lockout Voltage	$V_L$ Falling		3.6	3.8	V
Hysteresis			200		mV
<b>Error Amplifier</b>					
Unity-Gain BW Product	$V_{CC} = 5 \text{ V}$		10		MHz
Input Bias Current	$V_{NI} = V_{REF}, V_{FB} = 1.0 \text{ V}$	-1	0	1	$\mu\text{A}$
Offset Voltage	$V_{NI} = V_{REF}$	-15.0	0	15.0	mV
Output Current	Source ( $V_{FB} = 0.8 \text{ V}, NI = V_{REF}$ )			-1	mA
	Sink ( $V_{FB} = 2.4 \text{ V}, NI = V_{REF}$ )	0.8			
<b>PWR_GOOD</b>					
$V_{PWR\_GOOD}$ High	Typical Hysteresis = 1% $V_{NI} = V_{REF}$	$V_{NI} + 7\%$	$V_{NI} + 12\%$	$V_{NI} + 17\%$	V
$V_{PWR\_GOOD}$ Low		$V_{NI} - 17\%$	$V_{NI} - 12\%$	$V_{NI} - 7\%$	
Output Sink Current	$V_{DS} \leq 1 \text{ V}$	2			mA
<b>OVP</b>					
Threshold Voltage	$V_{NI} = V_{REF}$ $BST - L_X = 4.5 \text{ V}$	$V_{NI} + 12\%$	$V_{NI} + 17\%$	$V_{NI} + 22\%$	V
<b>OCP</b>					
$I_{CS}$ Sink Current	$4.75 \leq V_{ICS} \leq 13.2 \text{ V}$	126	170	204	$\mu\text{A}$

Notes

- a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

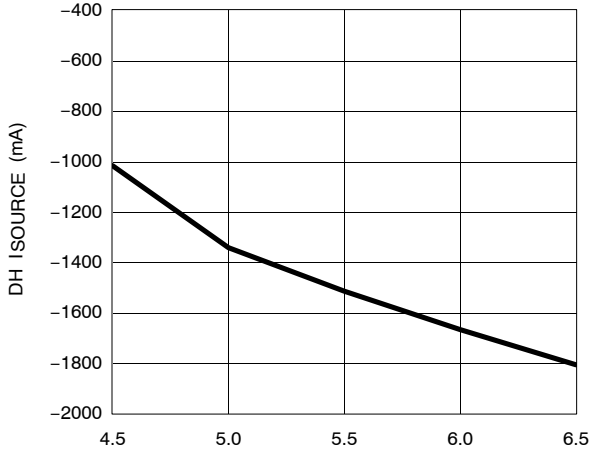
**TYPICAL CHARACTERISTICS (25 °C UNLESS OTHERWISE NOTED)**





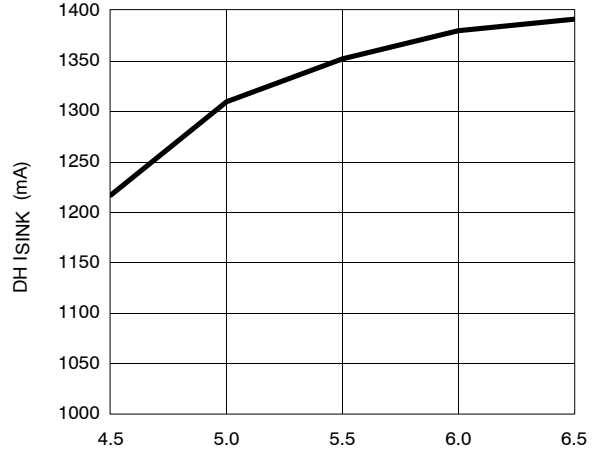
**TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)**

**DH I<sub>SOURCE</sub> vs. Voltage  
Between BST and LX**



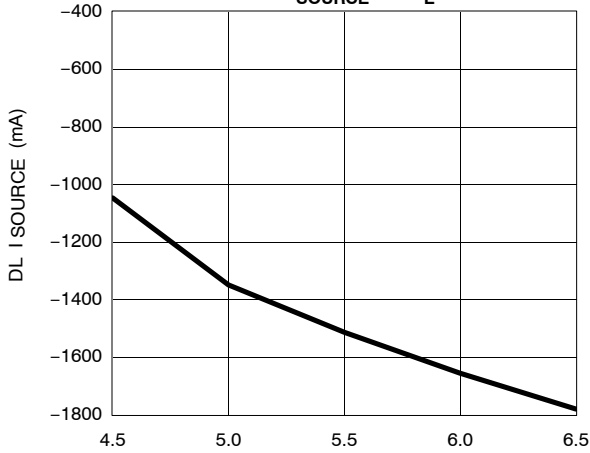
Voltage Between BST and LX (V)

**DH I<sub>SINK</sub> vs. Voltage  
Between BST and LX**



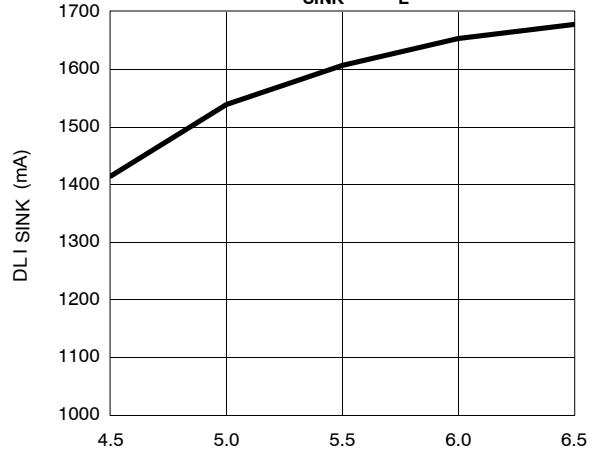
Voltage Between BST and LX (V)

**DL I<sub>SOURCE</sub> vs. V<sub>L</sub>**



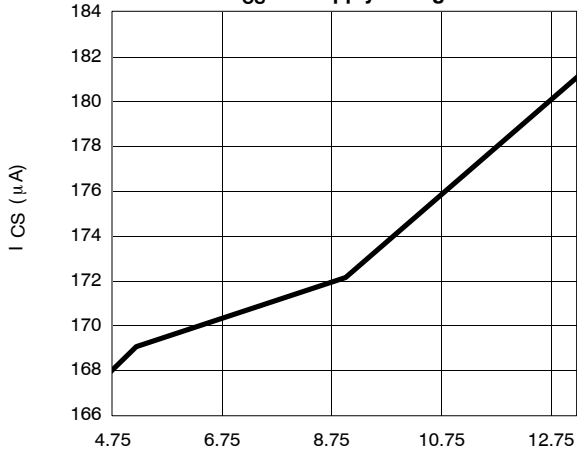
V<sub>L</sub> (V)

**DL I<sub>SINK</sub> vs. V<sub>L</sub>**



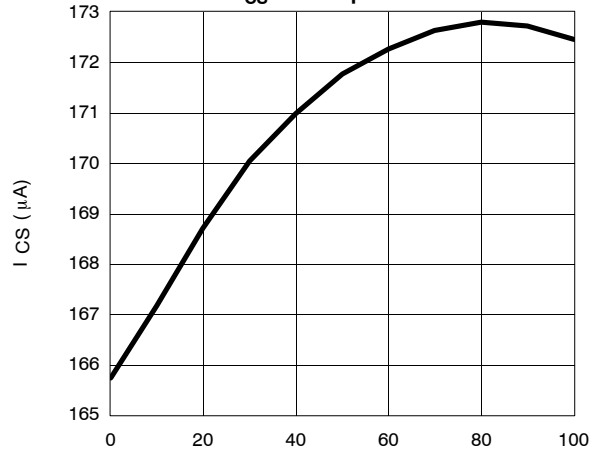
V<sub>L</sub> (V)

**I<sub>CS</sub> vs. Supply Voltage**

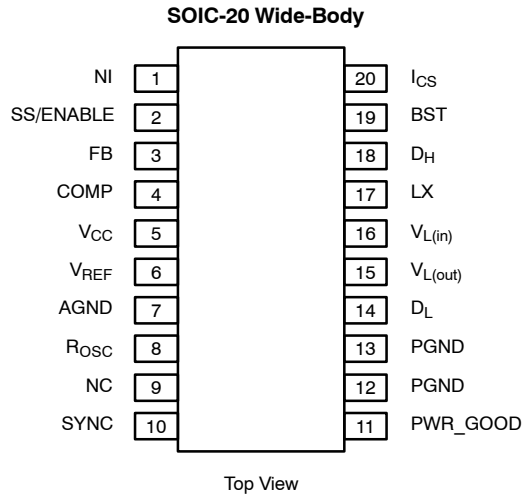


V<sub>DD</sub> - Supply Voltage (V)

**I<sub>CS</sub> vs. Temperature**



Temperature (C)

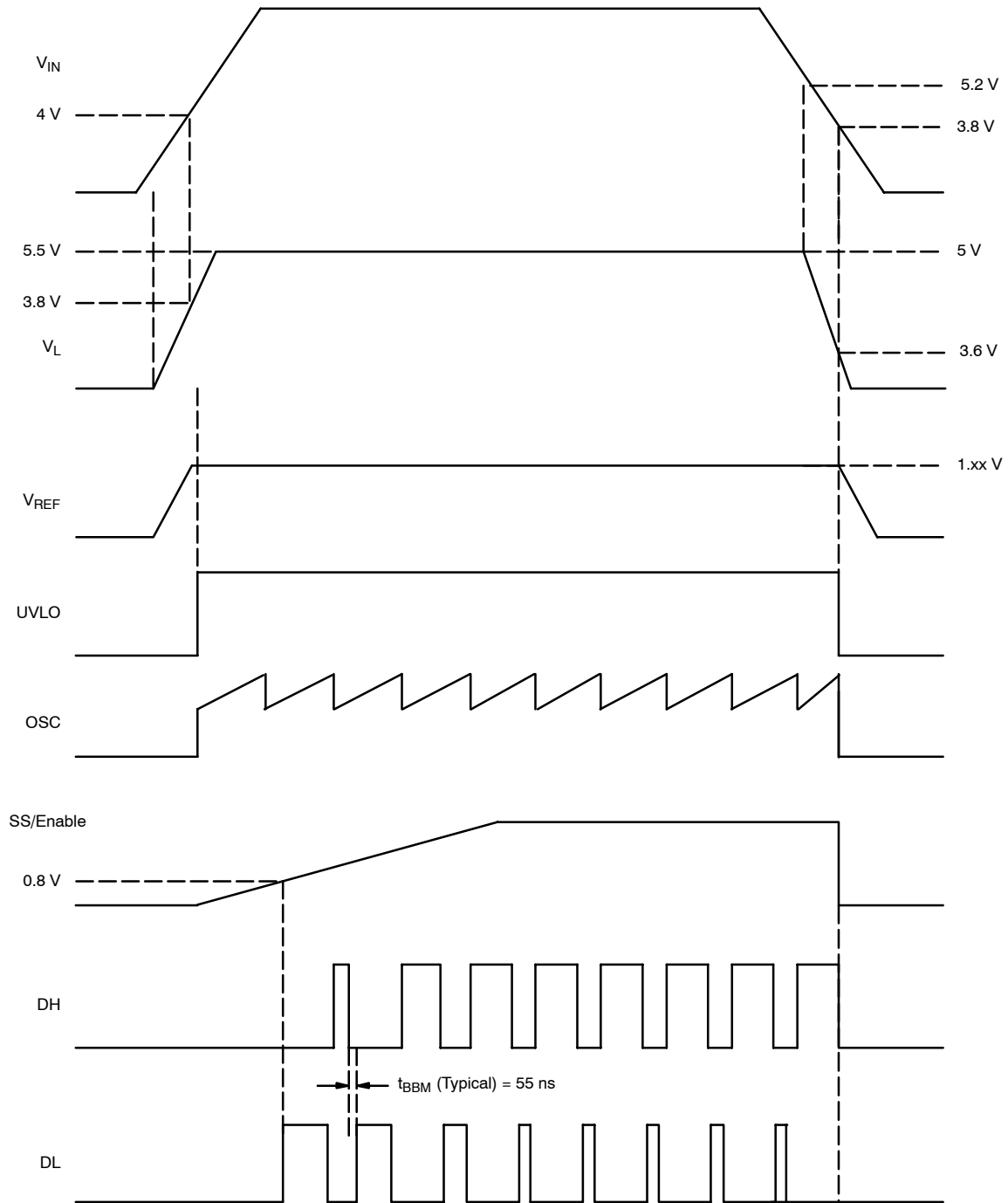

**PIN CONFIGURATION AND DESCRIPTION**

**ORDERING INFORMATION**

Part Number	Lead (Pb)-Free Part Number	Temperature Range	Packaging
Si9142CW		0 to 70°C	Bulk
Si9142CW-T1	Si9142CW-T1—E3		Tape and Reel

Ev Kit	Temperature Range	Board Type
Si9142 DB	0 to 70°C	Surface Mount

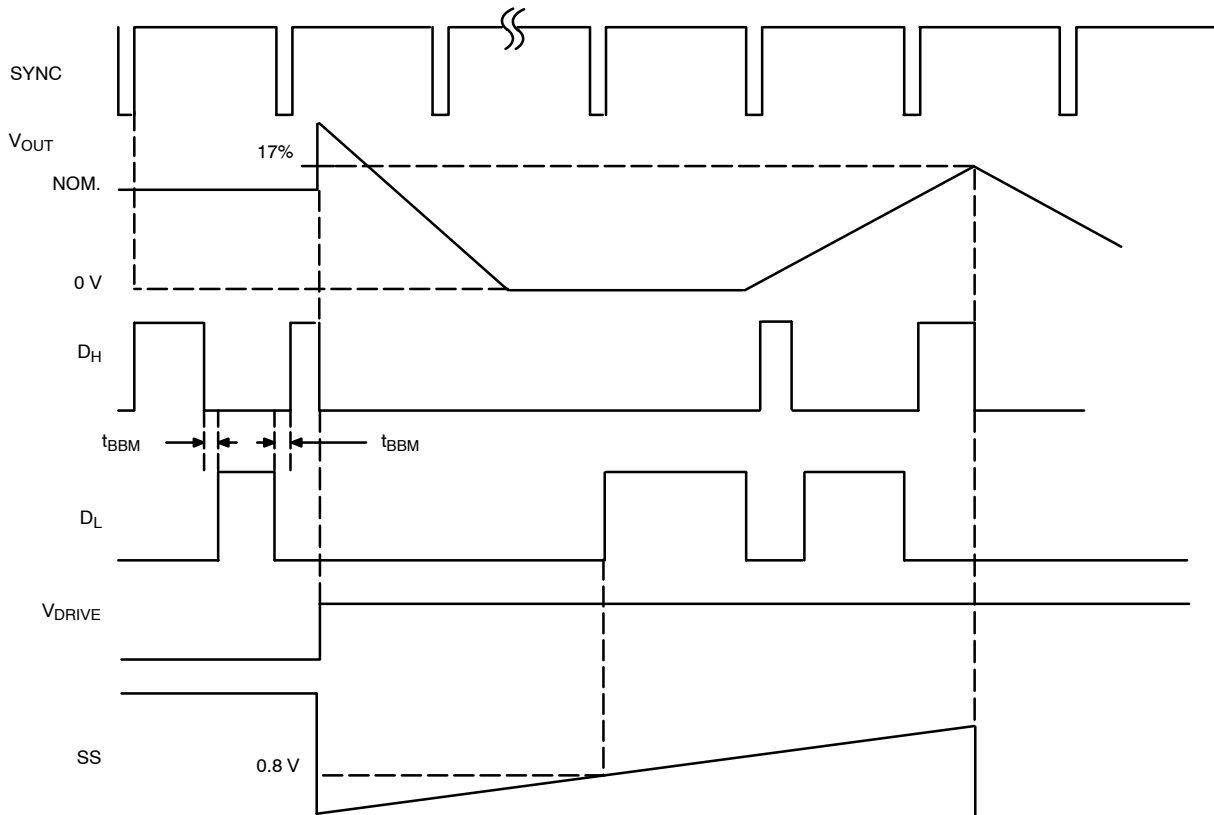
PIN NUMBER	SYMBOL	DESCRIPTION
1	NI	Error amplifier non-inverting input
2	SS/Enable	Soft-Start: Capacitor programmable or logic level controlled shutdown
3	FB	Feedback
4	COMP	Compensation node for the external feedback circuit
5	V <sub>CC</sub>	Input Voltage: 4.75 V to 13.2 V
6	V <sub>REF</sub>	1.30 V precision reference
7	AGND	Ground: Connect to quiet ground.
8	R <sub>OSC</sub>	External resistor to determine switching frequency
9	NC	Not internally connected
10	SYNC	Synchronizing Clock
11	PWR_GOOD	Power_Good window comparator output
12, 13	PGND	Power Ground
14	D <sub>L</sub>	Low-side gate driver for the synchronous rectifier
15	V <sub>L(out)</sub>	5.5-V reference for gate drive supply
16	V <sub>L(in)</sub>	Reference input, connect to RC filter from V <sub>L(out)</sub>
17	LX	Inductor connection node
18	D <sub>H</sub>	High-side gate driver for the power switch
19	BST	Boost capacitor connection node to generate high-side gate drive
20	I <sub>CS</sub>	Programmable over current limit

**TIMING DIAGRAMS**

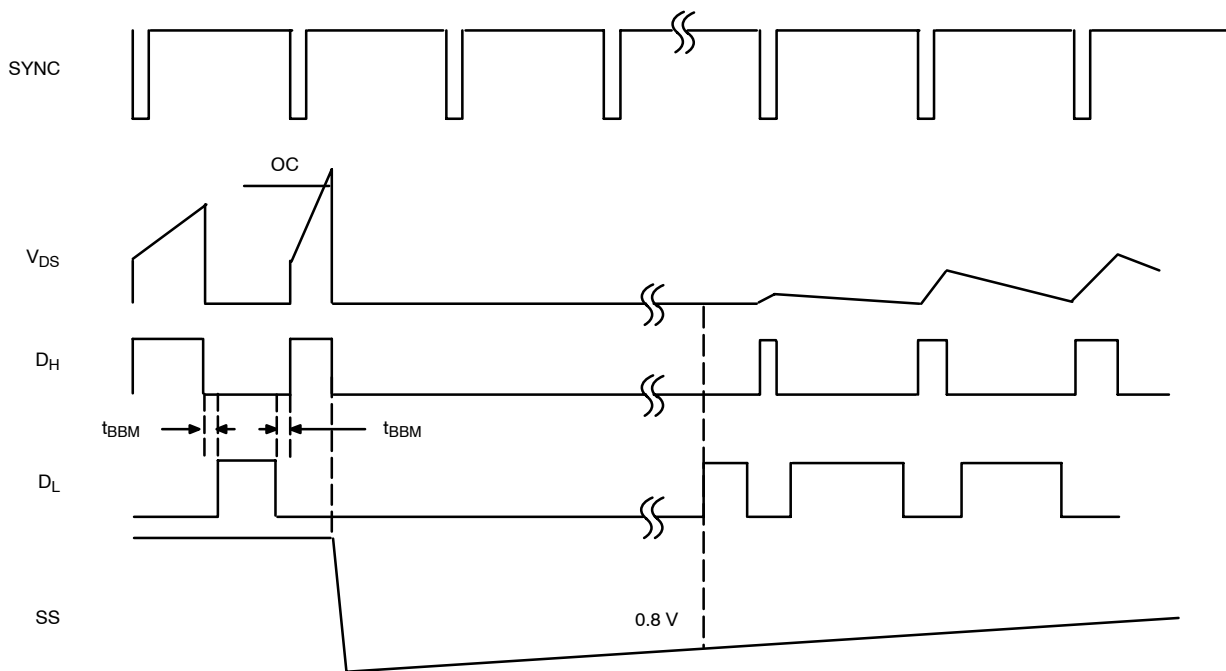


**FIGURE 1.** Start-up Timing Sequence

**TIMING DIAGRAMS (CONT'D)**



**FIGURE 2.** OVP Timing Diagram



**FIGURE 3.** OCP Timing Diagram



## DESCRIPTION OF OPERATION

The Si9142 is a voltage mode synchronous buck controller designed to power a high performance microprocessor power supply. The voltage mode control provides efficiency and cost saving advantages over current mode control in high output current converters by eliminating the current sense resistor. The Si9142 provides ultra-fast (5- $\mu$ sec) transient response time and all the necessary protection circuits demanded by microprocessor supply designers.

### Pin 1. NI – Non-Inverting Input

NI is the non-inverting input of the error amplifier. For converter output voltages equal to or greater than 1.3 V, the NI pin can be connected directly to  $V_{REF}$ . For converter output voltages less than 1.3 V, the NI pin can be connected to  $V_{REF}$  through a voltage divider.

### Pin 2. SS/Enable – Soft-Start/Enable

Soft-start is accomplished by connecting a capacitor from this pin to AGND. The soft-start functions as a constant current source into this capacitor. A logic low ( $\leq 0.8$  V) on this pin disables the output gate drives; the oscillator continues to function. A logic high ( $\geq 2.4$  V) enables the output gate drives, assuming the input voltage is above the UVLO threshold, and that no over-voltage or over-current condition exists.

### Pins 3 and 4. FB and COMP – Error Amplifier

FB is the inverting input of the error amplifier. The voltage on this pin is also connected internally to the input terminals of the OVP and PWR\_GOOD comparators for fault detection and protection. The error amplifier has 10-MHz gain-bandwidth when connected to a 20-pF load with 5-V input voltage. COMP is the output of the error amplifier. The output voltage is clamped at a maximum level to avoid long delays due to saturation during large transient conditions. The minimum COMP voltage is a diode drop below the 0% duty cycle voltage; the maximum voltage is a diode drop above the 94% duty cycle voltage.

### Pin 5. $V_{CC}$ – Input Voltage

The  $V_{CC}$  pin should be connected to the input voltage for optimum performance. The input voltage range of the Si9142 is specified to operate with either +5 VDC or +12 VDC. In order to accommodate the tolerance of the +12 V, and the possibility of using this controller in 2-cell Li+ notebook applications with a battery charger, the input voltage is rated up to +15-V absolute maximum.

### Pin 6. $V_{REF}$ – Reference Voltage

The reference voltage is designed to produce  $1.30\text{ V} \pm 1.6\%$  over the line and temperature range, to produce equally tight output regulation of the converter. The reference should be decoupled with at least 100-nF capacitance. The reference is capable of driving 1mA of external load.

### Pin 7. AGND – Analog Ground

AGND is the analog ground for the low power circuitry in the converter. This ground should be separated locally from PGND, and should have a separate run back to the input bypass capacitors.

### Pin 8. $R_{OSC}$ – Oscillator Timing Resistor

A resistor from this pin to AGND determines the internal switching frequency of the oscillator. The internal circuitry produces 10% frequency accuracy with a 1% timing resistor. The oscillator is capable of switching at up to 1 MHz.

### Pin 10. SYNC – Synchronization

The SYNC signal is generated from the internal oscillator. When the oscillator is ramping positive, SYNC will be logic high; when the oscillator is ramping negative, SYNC will be logic low. The SYNC pin can be used to synchronize the Si9142 to an external clock. In particular, if several Si9142s have their SYNC pins shorted together, they will all switch at the same frequency and in phase, with the frequency being set by the fastest oscillator.

### Pin 11. PWR\_GOOD – Open Collector Power Good Signal

This pin signals the status of the output voltage. The window comparator is set at  $\pm 12\%$  of the voltage at the NI pin, with a tolerance of 5%. The PWR\_GOOD signal is an open drain output capable of sinking 2 mA.

### Pins 12 and 13. PGND – Power Ground

PGND is the power ground for the high power circuitry in the converter. This ground should be separated locally from AGND, and should have a separate plane run back to the input bypass capacitors.

## DESCRIPTION OF OPERATION

### Pins 14 and 18. $D_L$ and $D_H$ – Low- and High-Side Gate Drives

$D_H$  is the high-side and  $D_L$  the low-side gate drive to the external MOSFETs. Both can source and sink 2.5-A peak with 4.5-V gate drives. The timing sequence of high- and low-side gate drives is shown in Figure 1. The internal break-before-make time interval ( $t_{BBM}$ ) of 55 nsec prevents shootthrough current in the external MOSFETs. The ringing from the gate drive output's trace inductance can produce negative voltages on  $D_H$  and  $D_L$  as much as 2-V negative with respect to PGND. The gate drive circuit is capable of withstanding these negative voltages without any functional defects.

### Pins 15 and 16. $V_{L(out)}$ and $V_{L(in)}$ – + 5.5-V Linear Regulator

$V_{L(out)}$  produces a + 5.5-V output used as the gate drive voltage for both the high- and low-side external MOSFETs. The gate drive voltage for the high-side MOSFET is bootstrapped ( $V_{L(out)} - V_{D(ODE)}$ ) above the input voltage.  $V_{L(out)}$  should be bypassed with at least 4.7  $\mu$ F of decoupling capacitance, and should not be used for any other external loads.  $V_{L(in)}$  drives the internal circuitry. It should be connected through an RC filter to  $V_{L(out)}$ .

### Pin 17. LX – Inductor Node

The LX node is used internally to float the high-side n-channel MOSFET gate drive. During the on-time of this MOSFET, the gate to source voltage will be ( $V_{L(out)} - V_{D(ODE)}$ ). The LX node is also used internally as the negative sense voltage for over-current protection.

### Pin 19. BST – Bootstrap Voltage

The external high-side n-channel MOSFET gate drive voltage is derived by bootstrapping the  $V_{L(out)}$  voltage on top of the input supply voltage. The external 100-nF capacitor connected across

the BST and LX pins is charged to ( $V_{L(out)} - V_{D(ODE)}$ ) when the external low-side MOSFETs are on. Then, when the low-side MOSFETs are turned off, BST is internally connected to  $D_H$  in order to turn on the high-side MOSFET.  $D_L$  is turned on at startup to ensure initial charging of the BST capacitor.

### Pin 20. ICS – Programmable Over-Current Protection

The over-current protection circuit senses the voltage across the external high-side n-channel MOSFET to determine the presence of an over-current condition. Current sensing occurs only during the on-time of this MOSFET. The trigger level of the over-current circuit is programmable by selecting the external resistor value connected from  $V_{CC}$  to ICS. Once the over-current circuit has been triggered, it disables both output gate drives within 250 nsec. The circuit also discharges the soft-start capacitor as shown in the timing diagram in Figure 3.

### Under Voltage Lock-Out (UVLO)

The internal UVLO circuit is designed to prevent a converter from starting when insufficient input voltage is present. UVLO disables the oscillator, soft-start and output drives of the Si9142 until  $V_{L(out)}$  reaches 3.8 V; see Figure 1. The UVLO circuit has 200-mV hysteresis to prevent turn-on and -off oscillations. When the oscillator is disabled, the Si9142 is in stand-by mode, and consumes only 150  $\mu$ A of supply current.

### Start-up Timing Sequence

Please refer to Figure 1 for this description. When  $V_{CC}$  reaches 4 V,  $V_{L(out)}$  produces at least 3.8 V, and  $V_{REF}$  has stabilized and is regulating. The UVLO circuit enables the oscillator and the soft-start circuits. Once the soft-start voltage exceeds 1.5 V, the gate drive pulses begin, with the duty cycle of the high-side MOSFET beginning at 0% and gradually increasing until the output voltage is in regulation.

**APPLICATIONS**

**Setting the Current Limit**

The current limit is set by comparing the voltage drop across the external high-side n-channel MOSFET with the voltage dropped across a sense resistor connected between V<sub>CC</sub> and I<sub>CS</sub>. The I<sub>CS</sub> pin draws a constant current, and thus the equation governing the overcurrent threshold is:

$$170 \mu\text{A} * R = I_{\text{Limit}} * R_{\text{MOSFET}}$$

Once the on-state resistance of the MOSFET is known, R can be selected to set the desired current limit. One caution is in order: since the MOSFET will normally be quite warm, the resistance used in the equation should be the maximum resistance at elevated temperatures, not typical resistance at 25°C. The designer should also leave adequate margin above the normal output current, both to account for tolerances and noise in the IC, as well as to permit any initial high currents while charging output capacitors.

**The Boost Diode**

The application circuit shows the use of a 1N4148 diode for the boost circuit. This provides a low-cost component for this

application. However, it may be advantageous in some circuits to use a Schottky diode instead. The difference is that the Schottky has less forward drop than the regular rectifier, and this in turn means a somewhat greater gate drive voltage for the external high-side MOSFET. For MOSFETs with high gate threshold and/or low transconductance, the additional gate drive may prove very beneficial in terms of the heating of the MOSFET, and in turn the efficiency of the converter. A 1/2-A, 30-V Schottky works well in this application.

**Grounding**

The Si9142 is provided with both analog and power ground pins (AGND and PGND, respectively). Because of the high gate drive currents the Si9142 can source, it is essential that these two grounds be separated. PGND should be attached to the source of the external low-side MOSFET; AGND should be attached to the small-signal components of the circuit, such as the timing resistor and the feedback resistor. Each of these grounds should be run back independently to the input line capacitors, to avoid ground loops.

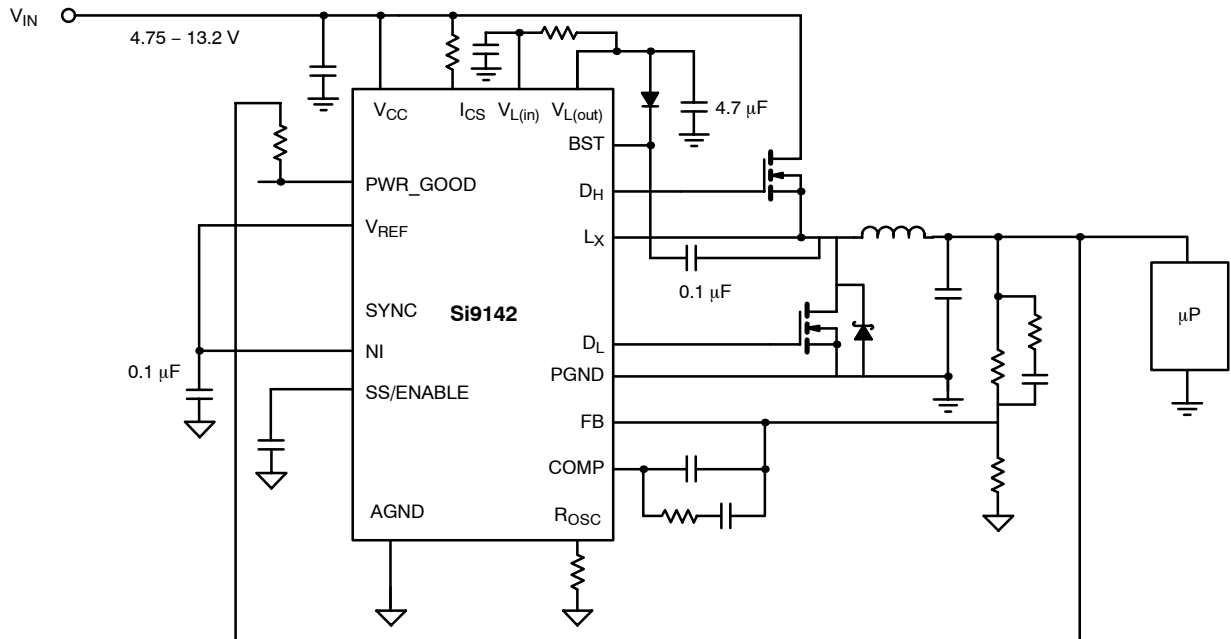


FIGURE 4. High Performance Converter



## Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.