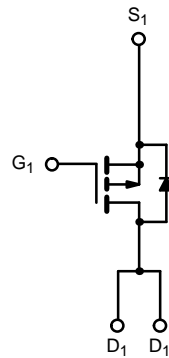
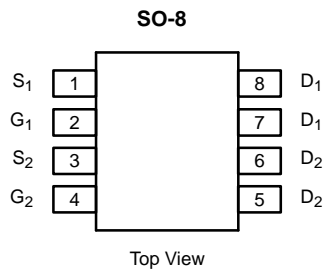




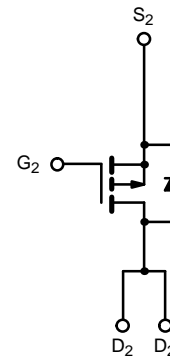
## Dual P-Channel 60-V (D-S), 175 °C MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
-60	0.17 @ $V_{GS} = -10$ V	$\pm 2.6$
	0.26 @ $V_{GS} = -4.5$ V	$\pm 2.1$

**175 °C Rated**  
Maximum Junction Temperature  
**TrenchFET®**  
Power MOSFETs



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175^\circ\text{C}$ ) <sup>a</sup>	$T_A = 25^\circ\text{C}$	$\pm 2.6$	A
	$T_A = 70^\circ\text{C}$	$\pm 2.2$	
Pulsed Drain Current	$I_{DM}$	$\pm 15$	
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	-2	
Maximum Power Dissipation <sup>a</sup>	$T_A = 25^\circ\text{C}$	2.4	W
	$T_A = 70^\circ\text{C}$	1.7	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typ	Max	Unit
Junction-to-Ambient <sup>a</sup>	$t \leq 10$ sec		62.5	$^\circ\text{C/W}$
	Steady State	$R_{thJA}$	93	

Notes

a. Surface Mounted on 1" x 1" FR4 Board

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>



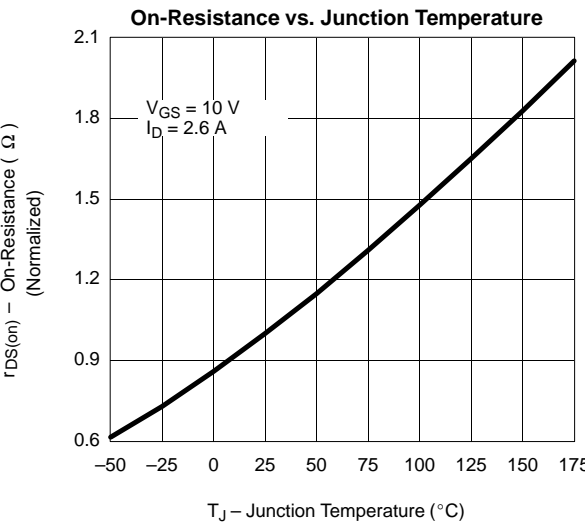
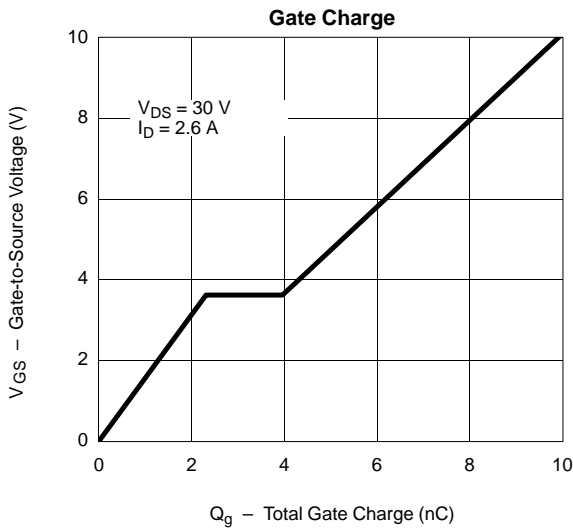
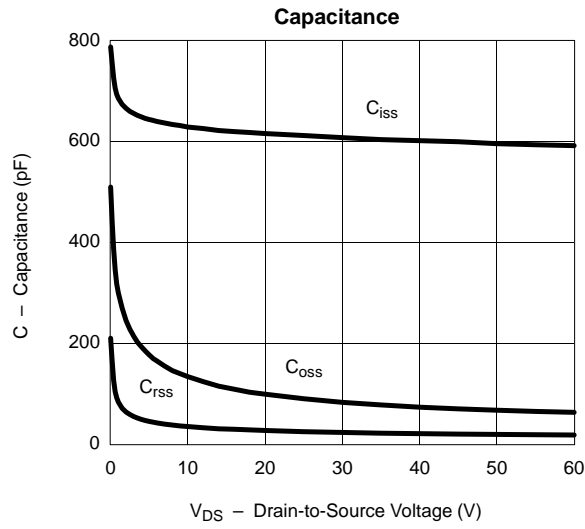
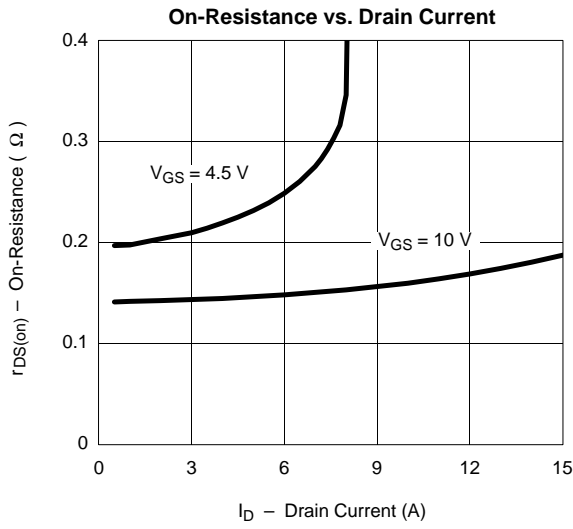
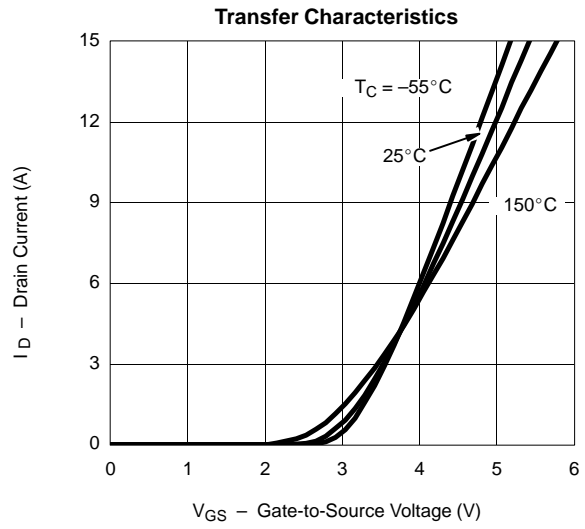
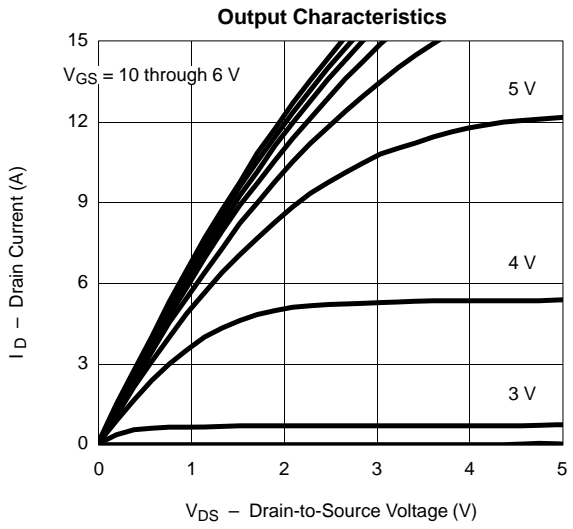
<b>SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)</b>						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-1			V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V			-1	μA
		V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C			-10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ -5 V, V <sub>GS</sub> = -10 V	-15			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -2.6 A		0.14	0.17	Ω
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -2.1 A		0.20	0.26	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -2.6 A		5.0		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = -2.0 A, V <sub>GS</sub> = 0 V			-1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -2.6 A		10	20	nC
Gate-Source Charge	Q <sub>gs</sub>			2.5		
Gate-Drain Charge	Q <sub>gd</sub>			1.8		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -30 V, R <sub>L</sub> = 30 Ω I <sub>D</sub> ≅ -1 A, V <sub>GEN</sub> = -10 V, R <sub>G</sub> = 6 Ω		8	20	ns
Rise Time	t <sub>r</sub>			10	20	
Turn-Off Delay Time	t <sub>d(off)</sub>			23	40	
Fall Time	t <sub>f</sub>			12	20	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = -2.0 A, di/dt = 100 A/μs		50	90	

Notes

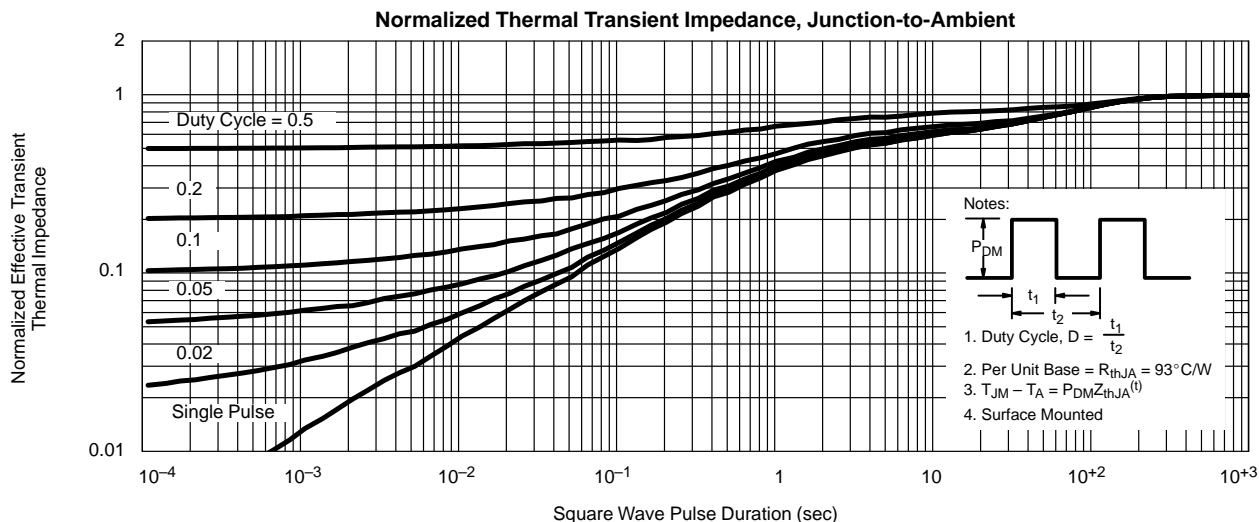
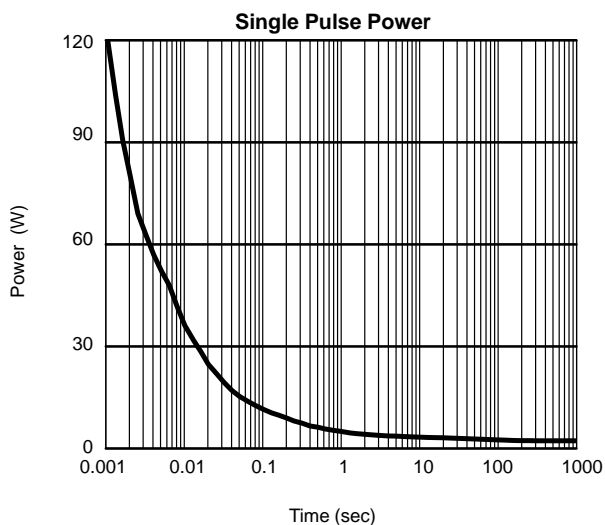
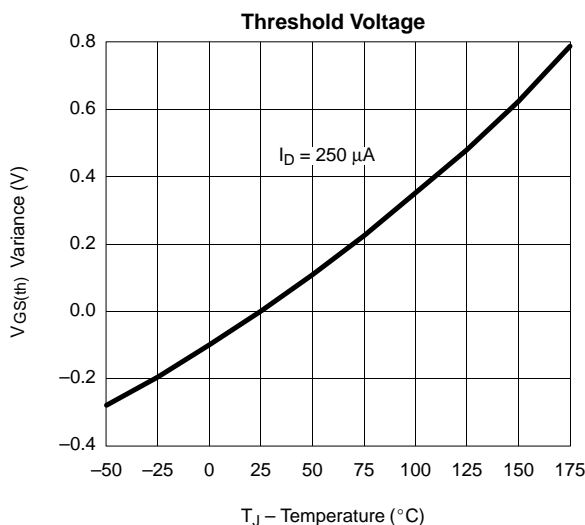
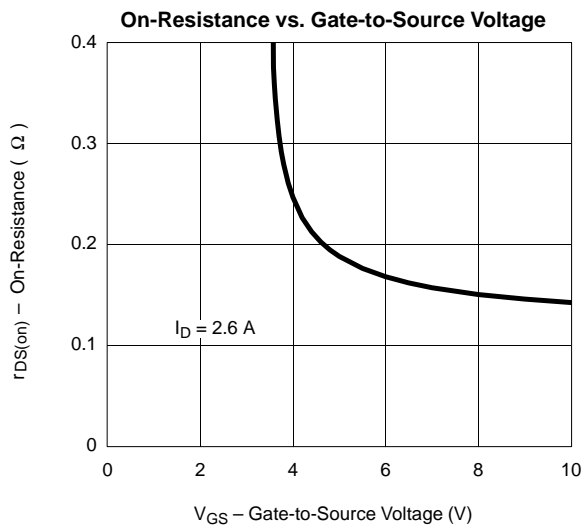
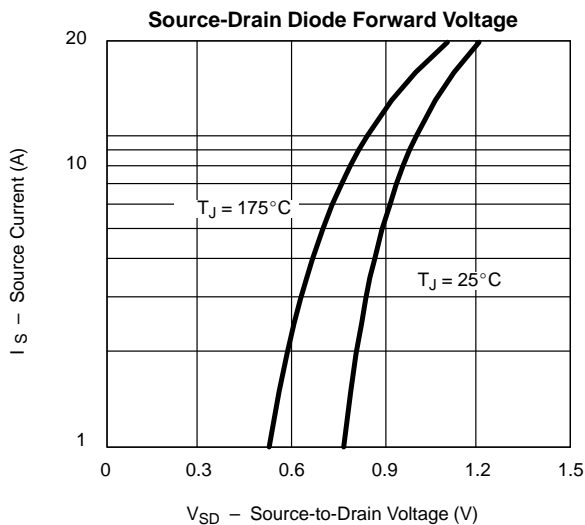
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**





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