



N-Channel 20-V (D-S), 175°C MOSFET

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



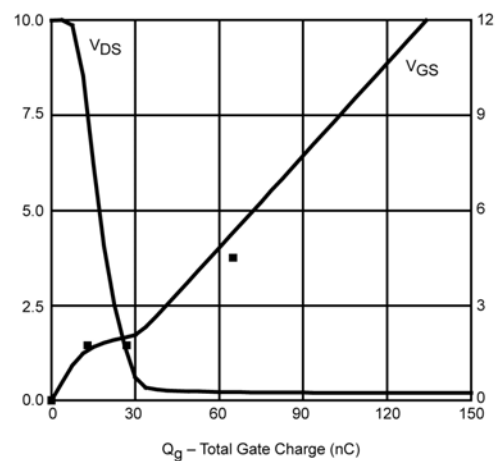
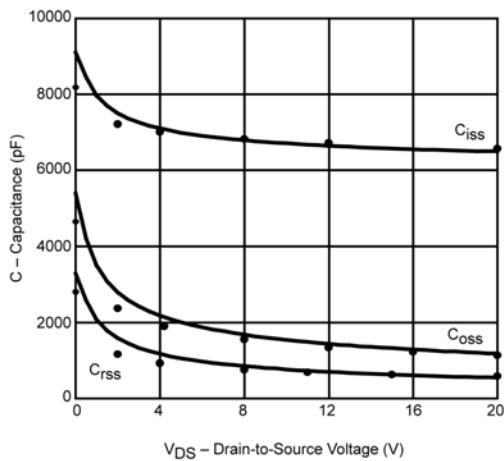
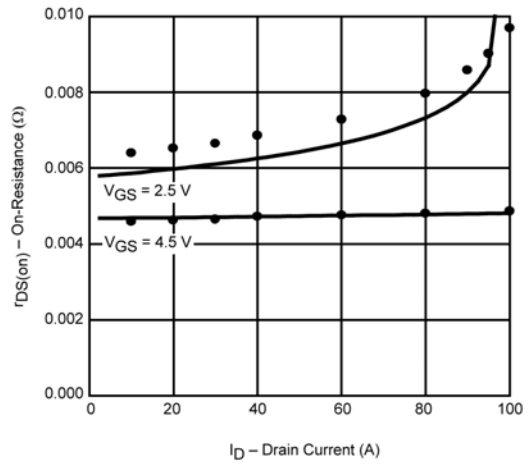
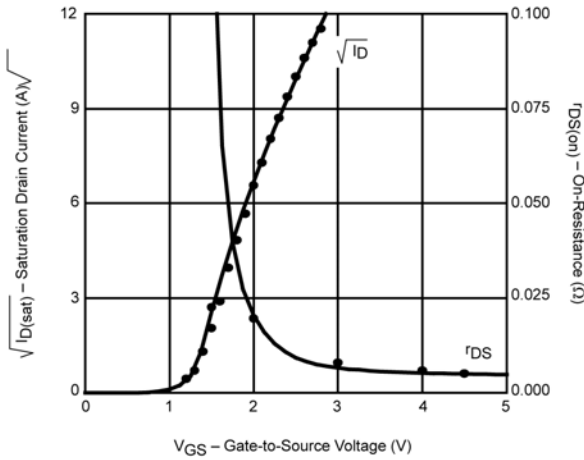
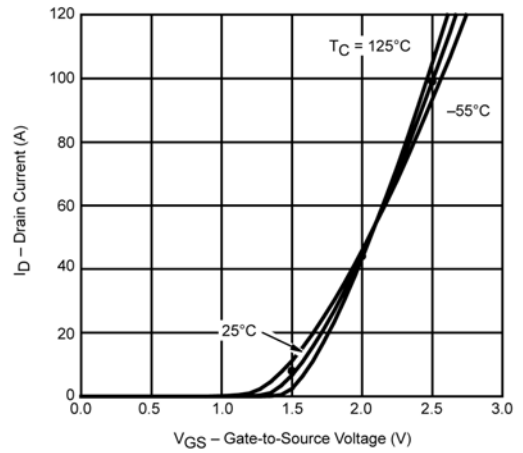
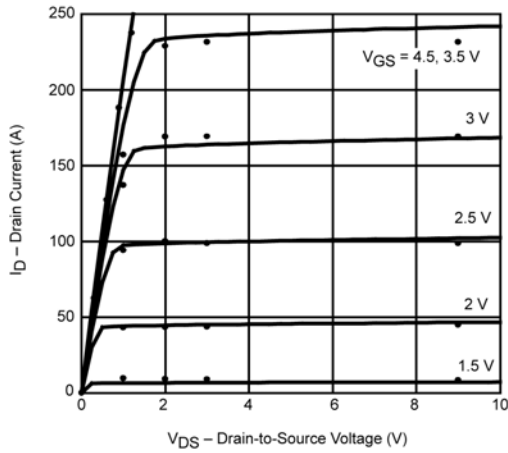
| SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED) | | | | | |
|---|---------------------|--|----------------|---------------|------|
| Parameter | Symbol | Test Condition | Simulated Data | Measured Data | Unit |
| Static | | | | | |
| Gate Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | 0.87 | | V |
| On-State Drain Current ^a | I _{D(on)} | V _{DS} = 5 V, V _{GS} = 4.5 V | 401 | | A |
| Drain-Source On-State Resistance ^a | r _{DS(on)} | V _{GS} = 4.5 V, I _D = 30 A | 0.0047 | | Ω |
| | | V _{GS} = 2.5 V, I _D = 20 A | 0.0059 | | |
| | | V _{GS} = 4.5 V, I _D = 30 A, T _J = 125°C | 0.0080 | | |
| | | V _{GS} = 4.5 V, I _D = 30 A, T _J = 175°C | 0.0091 | | |
| Forward Transconductance ^a | g _{fs} | V _{DS} = 5 V, I _D = 30 A | 85 | | S |
| Forward Voltage ^a | V _{SD} | I _S = 100 A, V _{GS} = 0 V | 0.93 | 1.2 | V |
| Dynamic^b | | | | | |
| Input Capacitance | C _{iss} | V _{GS} = 0 V, V _{DS} = 20 V, f = 1 MHz | 6499 | 6600 | pF |
| Output Capacitance | C _{oss} | | 1184 | 1150 | |
| Reverse Transfer Capacitance | C _{rss} | | 548 | 600 | |
| Total Gate Charge ^c | Q _g | V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 85 A | 57 | 65 | nC |
| Gate-Source Charge ^c | Q _{gs} | | 13 | 13 | |
| Gate-Drain Charge ^c | Q _{gd} | | 14 | 14 | |
| Turn-On Delay Time ^c | t _{d(on)} | V _{DD} = 10 V, R _L = 0.12 Ω I _D ≅ 85 A, V _{GEN} = 4.5 V, R _G = 2.5 Ω | 23 | 25 | ns |
| Rise Time ^c | t _r | | 43 | 120 | |
| Turn-Off Delay Time ^c | t _{d(off)} | | 81 | 80 | |
| Fall Time ^c | t _f | | 107 | 100 | |
| Reverse Recovery Time | t _{rr} | I _F = 50 A, di/dt = 100 A/μs | 55 | 100 | |

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



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