Bi-Directional P-Channel MOSFET/Power Switch

PRODUCT SUMMARY

<table>
<thead>
<tr>
<th>VDS (V)</th>
<th>$R_{DS(on)}$ (Ω)</th>
<th>$I_D$ (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>± 7</td>
<td>0.170 at $V_{GS} = -4.5$ V</td>
<td>± 2.4</td>
</tr>
<tr>
<td></td>
<td>0.240 at $V_{GS} = -2.5$ V</td>
<td>± 2.0</td>
</tr>
</tbody>
</table>

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Low $R_{DS(on)}$ Symmetrical P-Channel MOSFET
- Integrated Body Bias For Bi-Directional Blocking
- 2.5 V to 5.5 V Operation
- Exceeds ± 2 kV ESD Protected
- Solution for High-Side Battery Disconnect Switching (BDS)
- Supports Battery Switching in Multiple Battery Cell Phones, PDAs and PCS Products
- Low Profile, Small Footprint TSOP-6 Package
- Compliant to RoHS Directive 2002/95/EC

DESCRIPTION

The Si3831DV is a low on-resistance p-channel power MOSFET providing bi-directional blocking and conduction. Bi-directional blocking is facilitated by combining a 4-terminal symmetric p-channel MOSFET with a body bias selector circuit. Circuit operation automatically biases the p-channel body to the most positive source/drain potential thereby maintaining a reverse bias across the diode present between the source/drain terminals. Off-state device blocking characteristics are symmetric, facilitating bi-directional blocking for high-side battery switching in portable products. Gate drive is facilitated by negatively biasing the gate relative to the body potential. The off-state is achieved by biasing the gate to the most positive supply voltage or to the body potential. The Si3831DV is available in a 6-pin TSOP-6 package rated for the -25 °C to 85 °C commercial temperature range.

APPLICATION CIRCUITS

Note:

a. Patents pending.
Si3831DV
Vishay Siliconix

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

![Functional Block Diagram and Pin Configuration](image)

**Notes:**
- Bi-directional.
- Surface Mounted on FR4 board, \( t \leq 5 \) s.
- Surface Mounted on FR4 board, Steady-State.

**Figure 3.**

**Figure 4.**

**Ordering Information:**
- Si3831DV-T1-E3 (Lead (Pb)-free)
- Si3831DV-T1-GE3 (Lead (Pb)-free and Halogen-free)

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### ABSOLUTE MAXIMUM RATINGS \( T_A = 25 \degree C \), unless otherwise noted

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-Source Voltage, Source-Drain Voltage(^a)</td>
<td>( V_{DS} )</td>
<td>- 7.0 to + 7.0</td>
<td>V</td>
</tr>
<tr>
<td>Source-Body, Drain-Body, Gate-Body Voltage</td>
<td>( V_{SB}, V_{DB}, V_{GB} )</td>
<td>0.3 to - 7.0</td>
<td>V</td>
</tr>
<tr>
<td>Body-Substrate Voltage</td>
<td>( V_{BSUB} )</td>
<td>+ 7.0 to - 0.3</td>
<td>V</td>
</tr>
<tr>
<td>Continuous Drain-to-Source Current ( (T_J = 150 \degree C))(^a,b)</td>
<td>( I_D )</td>
<td>( \pm 2.4 )</td>
<td>A</td>
</tr>
<tr>
<td>( T_A = 25 \degree C )</td>
<td>( \pm 2.0 )</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>( T_A = 70 \degree C )</td>
<td>( \pm 2.0 )</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Pulsed Drain-to-Source Current(^b)</td>
<td>( I_{DM} )</td>
<td>( \pm 8 )</td>
<td>A</td>
</tr>
<tr>
<td>Maximum Power Dissipation(^b)</td>
<td>( P_D )</td>
<td>1.5</td>
<td>W</td>
</tr>
<tr>
<td>Operating Junction and Storage Temperature Range</td>
<td>( T_{J}, T_{stg} )</td>
<td>- 55 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

### RECOMMENDED OPERATING RANGE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Range</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-Source Voltage(^a)</td>
<td>( V_{DS} )</td>
<td>- 5.5 to 5.5</td>
<td>V</td>
</tr>
<tr>
<td>Gate-Drain, Gate-Source Voltage</td>
<td>( V_{GD}, V_{GS} )</td>
<td>0 to - 5.5</td>
<td>V</td>
</tr>
<tr>
<td>Source-Body, Drain-Body, Gate-Body Voltage</td>
<td>( V_{SB}, V_{DB}, V_{GB} )</td>
<td>0 to - 5.5</td>
<td>V</td>
</tr>
<tr>
<td>Drain-to-Source Current(^a,b)</td>
<td>( I_{DS} )</td>
<td>( \pm 2.4 )</td>
<td>A</td>
</tr>
<tr>
<td>Body-Source Current</td>
<td>( I_{BS} )</td>
<td>0 to 10</td>
<td>µA</td>
</tr>
</tbody>
</table>

### THERMAL RESISTANCE RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Junction-to-Ambient(^b)</td>
<td>( R_{thJA} )</td>
<td>80</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>125</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

**Notes:**
- \( a \): Bi-directional.
- \( b \): Surface Mounted on FR4 board, \( t \leq 5 \) s.
- \( c \): Surface Mounted on FR4 board, Steady-State.
**SPECIFICATIONS** $V_{BS} = 0$ V, $T_J = 25$ °C, unless otherwise noted

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate Threshold Voltage</td>
<td>$V_{GS(th)}$</td>
<td>$V_{DS} = V_{GS}$, $I_D = -250$ µA</td>
<td>- 0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Gate-Body Leakage</td>
<td>$I_{GS}$</td>
<td>$V_{DS} = 0$ V, $V_{GS} = -5.5$ V to $+0.3$ V</td>
<td>± 100</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current</td>
<td>$I_{DS}$</td>
<td>$V_{DS} = -5.5$ V, $V_{GS} = 0$ V, $V_{SB} = 0$ V</td>
<td></td>
<td>- 1</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>On-State Drain Current</td>
<td>$I_{D(on)}$</td>
<td>$V_{DS} = -3$ V, $V_{GS} = -4.5$ V</td>
<td>- 8</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Drain-Source On-State Resistance</td>
<td>$R_{DS(on)}$</td>
<td>$V_{GS} = -4.5$ V, $I_D = -2.4$ A</td>
<td>0.130</td>
<td>0.170</td>
<td>0.240</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DS} = -5.5$ V, $V_{GS} = 0$ V, $V_{SB} = 0$ V, $T_J = 70$ °C</td>
<td></td>
<td>- 5</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Dynamic</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Gate Charge</td>
<td>$Q_g$</td>
<td>$V_{DS} = -5$ V, $V_{GS} = -4.5$ V, $I_D = -2.4$ A</td>
<td>2.0</td>
<td>4.0</td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>Gate-Source Charge</td>
<td>$Q_{gs}$</td>
<td></td>
<td>0.23</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate-Drain Charge</td>
<td>$Q_{gd}$</td>
<td></td>
<td>0.14</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-On Delay Time</td>
<td>$t_{d(on)}$</td>
<td></td>
<td>12</td>
<td>25</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Rise Time</td>
<td>$t_r$</td>
<td>$V_{DD} = -3$ V, $R_L = 3$ Ω, $I_D = -1.0$ A, $V_{GEN} = -4.5$ V, $R_g = 6$ Ω</td>
<td>55</td>
<td>110</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-Off Delay Time</td>
<td>$t_{d(off)}$</td>
<td></td>
<td>90</td>
<td>180</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fall Time</td>
<td>$t_f$</td>
<td></td>
<td>85</td>
<td>170</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes:
- a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**GATE BUFFER REFERENCE**

**Figure 5. Gate Buffer Referenced to Most Positive Supply**

**Figure 6. Gate Buffer Referenced to Body Bias Pin**
TYPICAL CHARACTERISTICS  25 °C, unless otherwise noted

**Output Characteristics**

- **On-Resistance vs. Drain Current**
  - $V_{GS} = 5 \text{ V thru } 3 \text{ V}$
  - $V_{GS} = 2.5 \text{ V}$
  - $V_{GS} = 2 \text{ V}$
  - $V_{GS} = 1.5 \text{ V}$
  - $V_{GS} = 1 \text{ V}$

- **Gate Charge**
  - $V_{DS} = 3 \text{ V}$
  - $I_{D} = 2.4 \text{ A}$

**Transfer Characteristics**

- **Capacitance**
  - $C_{oss}$
  - $C_{iss}$
  - $C_{rss}$

- **On-Resistance vs. Junction Temperature**
  - $T_{J} = -55 \text{ °C}$
  - $25 \text{ °C}$
  - $125 \text{ °C}$

- **Gate Charge**
  - $Q_{G}$ - Total Gate Charge (nC)

- **On-Resistance vs. Drain Current**
  - $R_{DS(on)}$

- **Capacitance**
  - $V_{DS}$ - Drain-to-Source Voltage (V)
  - $V_{GS}$ - Gate-to-Source Voltage (V)

- **On-Resistance vs. Junction Temperature**
  - $V_{GS}$ - Gate-to-Source Voltage (V)
  - $I_{D}$ - Drain Current (A)
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

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**Source-Drain Diode Forward Voltage**

- Voltage ($V_{SD}$) vs. Current ($I_S$) at different temperatures ($T_J$):
  - $T_J = 150 °C$
  - $T_J = 25 °C$

**Threshold Voltage**

- Voltage ($V_{GS(th)}$) vs. Current ($I_D$) at $T_J = 25 °C$ and $T_J = 150 °C$:
  - $I_D = 0.5 A$
  - $I_D = 2.4 A$

**On-Resistance vs. Gate-to-Source Voltage**

- Resistance ($R_{DS(on)}$) vs. Voltage ($V_{GS}$) for $I_D = 250 \mu A$, $I_D = 2.4 A$.

**Normalized Thermal Transient Impedance**

- Impedance vs. Pulse Duration ($t_1$, $t_2$) and Duty Cycle ($D$).

**Normalized Effective Transient Thermal Impedance**

- Impedance vs. Pulse Duration ($t_1$, $t_2$) and Duty Cycle ($D$).

**Single Pulse Power**

- Power vs. Time ($t_1$, $t_2$) for Duty Cycle $D = 0.5$.

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**Notes:**

1. Duty Cycle, $D = \frac{t_1}{t_1 + t_2}$
2. Per Unit Base = $P_{RJA} = 80 °C/W$
3. $T_{JM} = T_A = P_{RJA}A_{JA}^{0.6}$
4. Surface Mounted
TYPICAL CHARACTERISTICS  25 °C, unless otherwise noted

Bi-Directional Blocking Drain-Source Voltage

V_{DG} = -2.5 V
V_{GB} = 0 V
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