



### N-Channel 2.5-V (G-S) MOSFET

#### CHARACTERISTICS

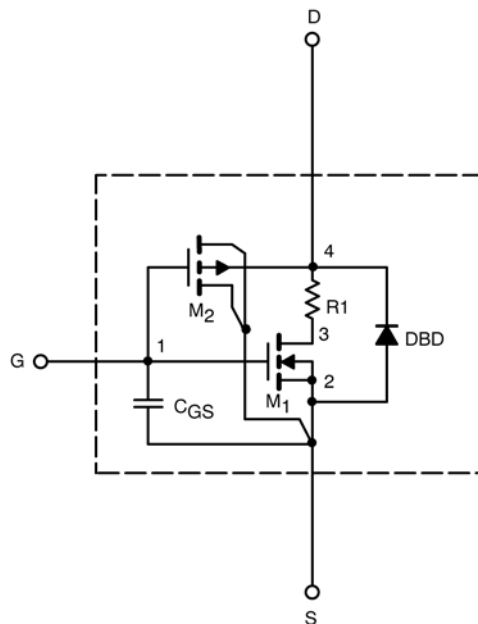
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

#### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



| SPECIFICATIONS ( $T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED) |              |  |  |               |          |
|---|--------------|--|--|---------------|----------|
| Parameter   | Symbol       | Test Condition   | Simulated Data   | Measured Data | Unit     |
| <b>Static</b>   |              |  |  |               |          |
| Gate Threshold Voltage  | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 1.2 \text{ mA}$  | 0.98   |               | V        |
| On-State Drain Current <sup>a</sup>                               | $I_{D(on)}$  | $V_{DS} \geq 5 \text{ V}, V_{GS} = 4.5 \text{ V}$  | 185  |               | A        |
| Drain-Source On-State Resistance <sup>a</sup>                     | $r_{DS(on)}$ | $V_{GS} = 4.5 \text{ V}, I_D = 6.9 \text{ A}$  | 0.016  | 0.017         | $\Omega$ |
|   |              | $V_{GS} = 2.5 \text{ V}, I_D = 2 \text{ A}$  | 0.020  | 0.021         |          |
| Forward Transconductance <sup>a</sup>                             | $g_{fs}$     | $V_{DS} = 10 \text{ V}, I_D = 6.9 \text{ A}$   | 32   | 30            | S        |
| Diode Forward Voltage <sup>a</sup>                                | $V_{SD}$     | $I_S = 1.1 \text{ A}, V_{GS} = 0 \text{ V}$  | 0.72   | 0.70          | V        |
| <b>Dynamic<sup>b</sup></b>  |              |  |  |               |          |
| Total Gate Charge   | $Q_g$        | $V_{DS} = 6 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 6.9 \text{ A}$  | 12.3   | 13.7          | nC       |
| Gate-Source Charge  | $Q_{gs}$     |  | 2.3  | 2.3           |          |
| Gate-Drain Charge   | $Q_{gd}$     |  | 4.1  | 4.1           |          |
| Turn-On Delay Time  | $t_{d(on)}$  | $V_{DD} = 6 \text{ V}, R_L = 6 \Omega$<br>$I_D \cong 1 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_G = 6 \Omega$ | 22   | 17            | Ns       |
| Rise Time   | $t_r$        |  | 30   | 46            |          |
| Turn-Off Delay Time   | $t_{d(off)}$ |  | 34   | 54            |          |
| Fall Time   | $t_f$        |  | 51   | 29            |          |
| Source-Drain Reverse Recovery Time                                | $t_{rr}$     |  | $I_F = 1.1 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ | 61            |          |

**Notes**

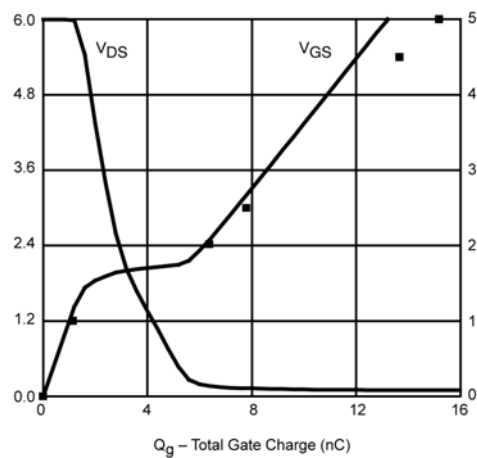
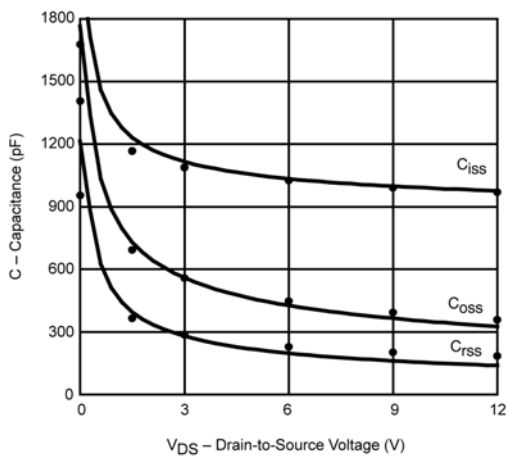
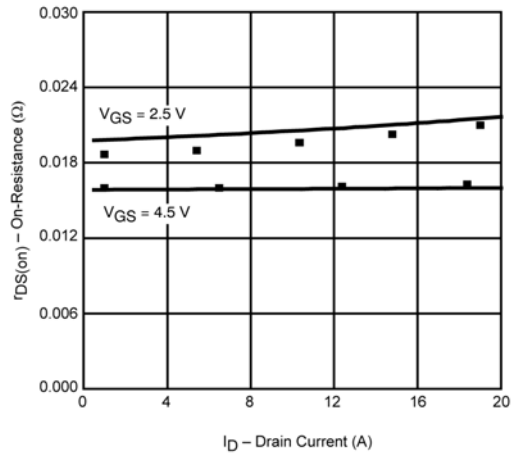
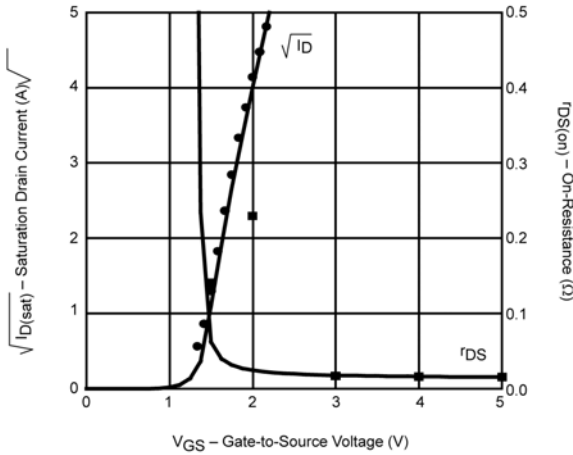
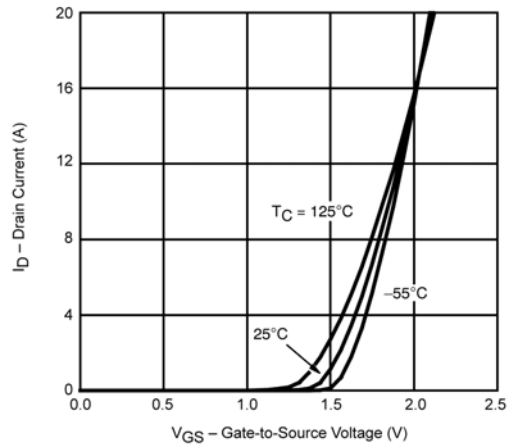
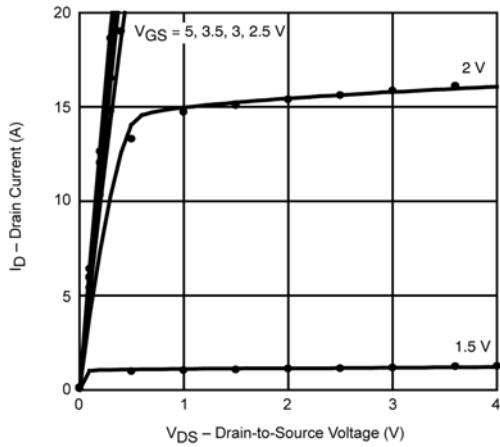
- a. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.



# SPICE Device Model Si5406DC

## Vishay Siliconix

COMPARISON OF MODEL WITH MEASURED DATA ( $T_J=25^\circ\text{C}$  UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



## Disclaimer

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