



### N-Channel Enhancement-Mode MOSFET, 4-mΩ $r_{DS(on)}$

#### CHARACTERISTICS

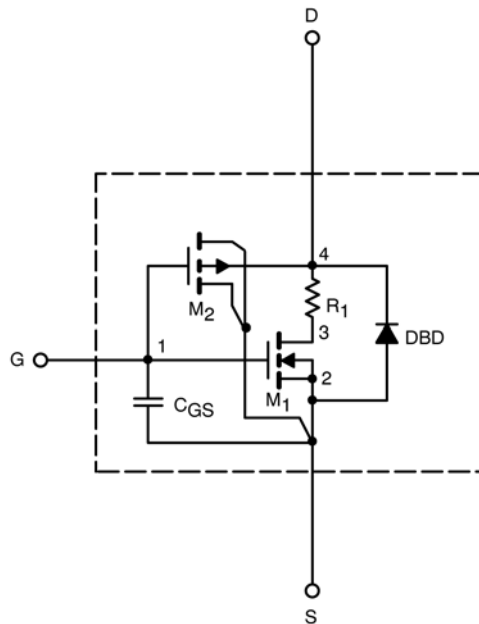
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

#### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



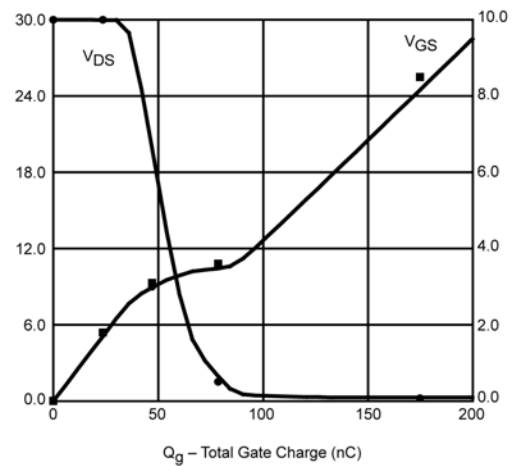
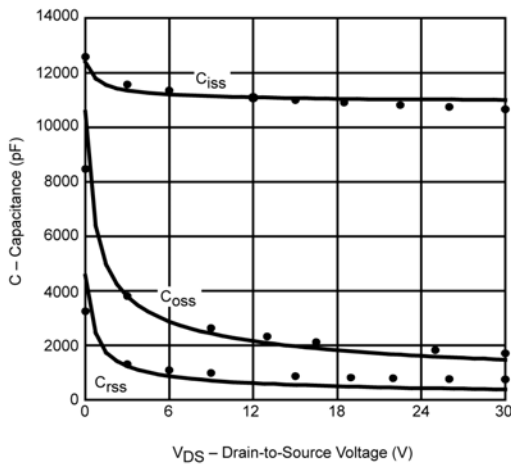
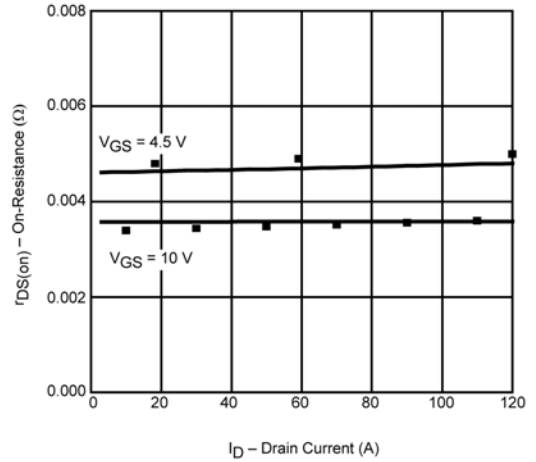
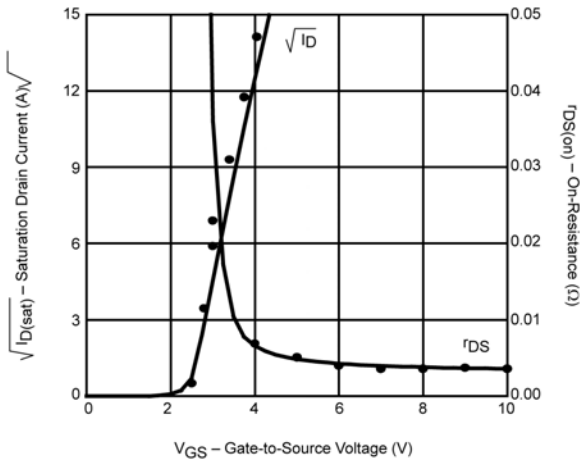
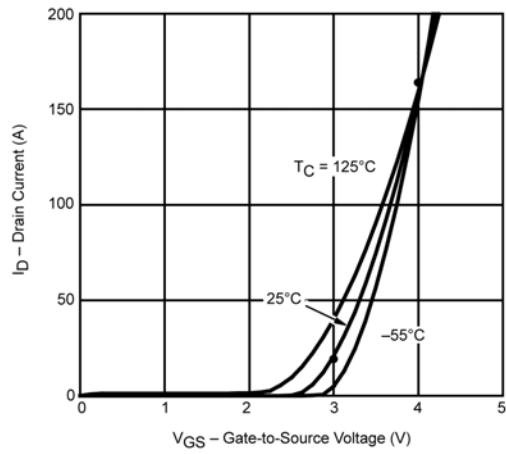
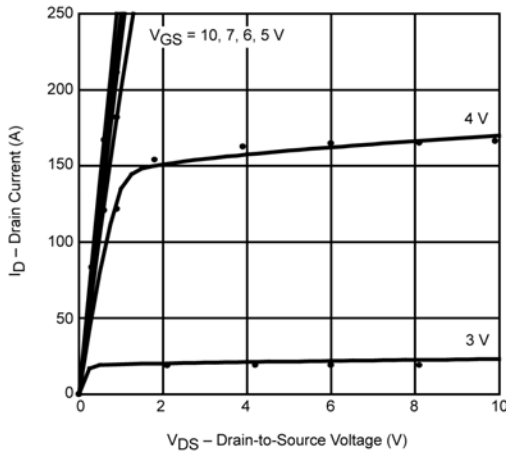
SPECIFICATIONS (T <sub>J</sub> = 25°C UNLESS OTHERWISE NOTED)				
Parameter	Symbol	Test Condition	Typical	Unit
<b>Static</b>				
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.64	V
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	1340	A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 75 A	0.0035	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 75 A	0.0052	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 25 A, T <sub>J</sub> = 125°C	0.005	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 25 A, T <sub>J</sub> = 175°C	0.006	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 25 A	72	S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = I <sub>S</sub> = 75 A, V <sub>GS</sub> = 0 V	0.92	V
<b>Dynamic</b>				
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz	11020	pF
Output Capacitance	C <sub>oss</sub>		1606	
Reverse Transfer Capacitance	C <sub>rss</sub>		436	
Total Gate Charge <sup>b</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 75 A	190	nC
Gate-Source Charge <sup>b</sup>	Q <sub>gs</sub>		40	
Gate-Drain Charge <sup>b</sup>	Q <sub>gd</sub>		40	
Turn-On Delay Time <sup>b, c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 6 Ω I <sub>D</sub> ≅ 50 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 2.5 Ω	38	ns
Rise Time <sup>b, c</sup>	t <sub>r</sub>		40	
Turn-Off Delay Time <sup>b, c</sup>	t <sub>d(off)</sub>		228	
Fall Time <sup>b, c</sup>	t <sub>f</sub>		61	
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 50 A, di/dt = 100 A/μs	63	A
	I <sub>RM(rec)</sub>		0.81	
	Q <sub>rr</sub>		0.26	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.



COMPARISON OF MODEL WITH MEASURED DATA ( $T_J=25^\circ\text{C}$  UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



## Disclaimer

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