



Dual N-Channel 2.5 V (G-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)		
20	0.075 at V _{GS} = 4.5 V	± 4.2		
	0.134 at V _{GS} = 2.5 V	± 3.1		

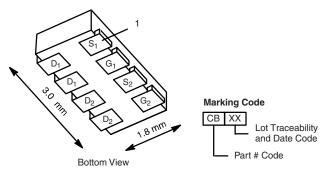
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET: 2.5 V Rated
- Compliant to RoHS Directive 2002/95/EC



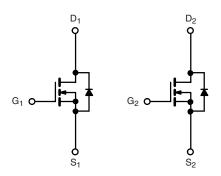


1206-8 ChipFET®



Ordering Information: Si5904DC-T1-E3 (Lead (Pb)-free)

Si5904DC-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted							
Parameter		Symbol	5 s	Steady State	Unit		
Drain-Source Voltage		V _{DS}	20		V		
Gate-Source Voltage		V _{GS}	± 12				
Continuous Drain Current /T 150 °C\2	T _A = 25 °C	- I _D	± 4.2	± 3.1			
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 85 °C		± 3.0	± 2.2	Δ.		
Pulsed Drain Current		I _{DM}	± 10		Α		
Continuous Source Current (Diode Conduction) ^a		I _S	1.8	0.9			
Mariana Barra Biratanting	T _A = 25 °C	P _D	2.1	1.1	W		
Maximum Power Dissipation ^a	T _A = 85 °C		1.1	0.6	VV		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C		
Soldering Recommendations (Peak Temperature) ^{b, c}			260				

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Marrian Incation to Ambient	t ≤ 5 s	R _{thJA}	50	60		
Maximum Junction-to-Ambient ^a	Steady State		90	110	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	30	40		

Notes:

- a. Surface mounted on 1" x 1" FR4 board.
- b. See reliability manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

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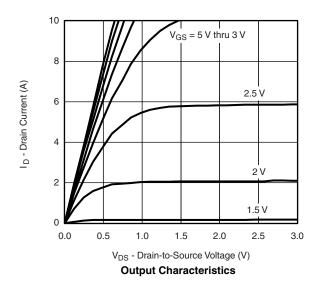
SPECIFICATIONS T _J = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions Min.		Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.6		1.5	V	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA	
Zava Cata Valtaga Dvain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			1	μΑ	
Zero Gate Voltage Drain Current		$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 85 ^{\circ}\text{C}$			5		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	10			Α	
D : 0	D	$V_{GS} = 4.5 \text{ V}, I_D = 3.1 \text{ A}$		0.065	0.075	0	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 2.5 \text{ V}, I_D = 2.3 \text{ A}$		0.115	0.143	Ω	
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 10 \text{ V}, I_D = 3.1 \text{ A}$		8		S	
Diode Forward Voltage ^a	V_{SD}	I _S = 0.9 A, V _{GS} = 0 V		0.8	1.2	V	
Dynamic ^b							
Total Gate Charge	Q_g			4	6		
Gate-Source Charge	Q_{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 3.1 \text{ A}$		0.6		nC	
Gate-Drain Charge	Q_{gd}			1.3			
Turn-On Delay Time	t _{d(on)}			12	18		
Rise Time	t _r	V_{DD} = 10 V, R_L = 10 Ω		35	55	ns	
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ 1 A, V_{GEN} = 4.5 V, R_g = 6 Ω		19	30		
Fall Time	t _f			9	15		
Source-Drain Reverse Recovery Time	t _{rr}	$I_F = 0.9 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}$		40	80		

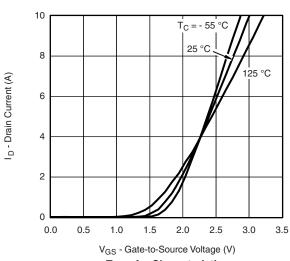
Notes:

- a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



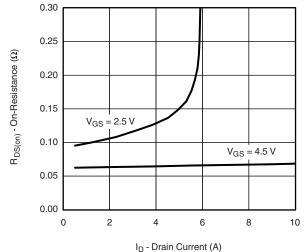


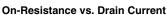


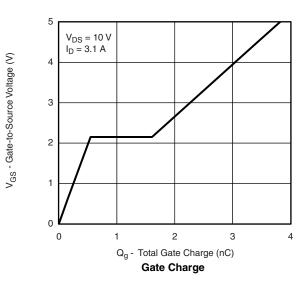


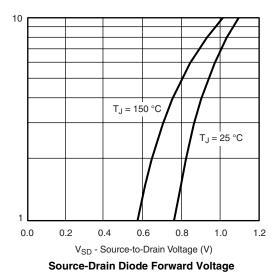


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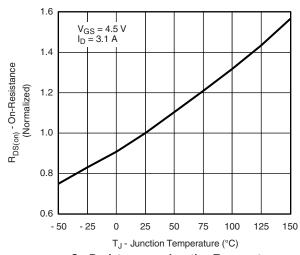




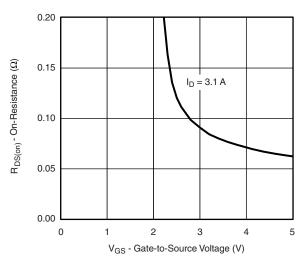


600
500
Ciss
400
300
100
Coss
Crss
Crss
100
0
4 8 12 16 20

V_{DS} - Drain-to-Source Voltage (V) **Capacitance**



On-Resistance vs. Junction Temperature



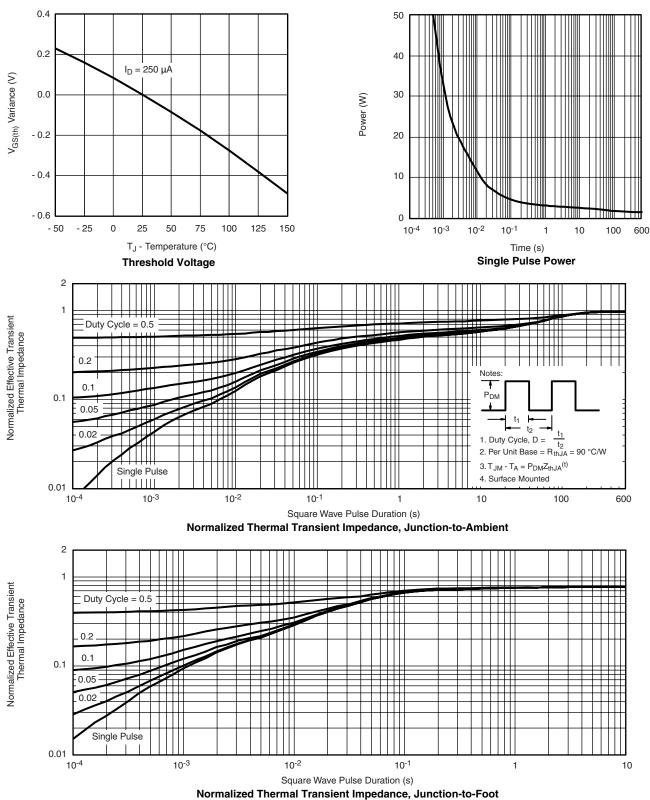
On-Resistance vs. Gate-to-Source Voltage

Is - Source Current (A)

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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