# Designing A Flyback Converter with Si9113 for Feeding the TE from U-Interface In ISDN

*Nitin Kalje and Tony Lai*

## INTRODUCTION

The efficiency of the converter powering the NT is extremely important, even at power levels of a few milliwatts. To achieve 60% efficiency with an 80-mW output, the allowable power loss in the converter is less than 54 mW. The components of these losses include the dc and switching losses in the semiconductors, the transformer, quiescent current overhead in the control chip, current and voltage sense networks, power losses from the ripple current through the input and output capacitor ESR, resistive losses in the PCB traces, and any external control circuit operating losses. Built on a proprietary BiC/DMOS technology, the Si9113 integrates all the functions necessary to minimize power consumption. Its major features include:

- programmable start/stop
- less than 5-μA supply current in UVLO mode
- internal start-up circuit, programmable soft-start, and power_good output.

The following sections discuss in detail design considerations for creating an efficient 800-mW flyback converter with the Si9113. Refer to the application circuit from Figure 6.

### Start/Stop Programming

The European Telecommunication Standards Institute (ETSI) requires the NT1 and the regenerator directed towards the line terminal to remain at a high impedance state for as long as the input line voltage stays below 18 V. The high impedance state is defined by the maximum leakage current through the equipment and its minimum input capacitance. In this state the leakage current must be less than 10 μA and the capacitance more than 1 μF.

The Si9113 includes a very high input impedance-window comparator, which can be programmed to set an accurate undervoltage lockout (UVLO) level with adequate hysteresis. The programmable hysteresis avoids unintentional locking of the system during start up, especially when the system is fed from long loops of telephone line. The comparators need a mere 0.05-μA input bias current. Moreover, when in UVLO mode, the Si9113 disables the internal reference generator, soft-start, oscillator circuit, and most of the control section to reduce the supply current below 5 μA. This keeps the total current drawn by the converter below 10 μA and meets the ETSI standard. See Figure 1 for the current behavior of the Si9113 with respect to the input voltage. When the converter is on, the $V_{CC}$ is supplied by the boot-strap winding and the internal depletion MOSFET opens.

Figure 2 shows how the hysteresis is achieved. Refer to equations 1 and 2 to calculate the resistor values for proper undervoltage lockout and the hysteresis.

$$V_{START} = \frac{R3 + R4 + R5}{R5} \times 8.8 \quad (1)$$

$$V_{STOP} = \frac{R3 + R5}{R5} \times 8.8 \quad (2)$$

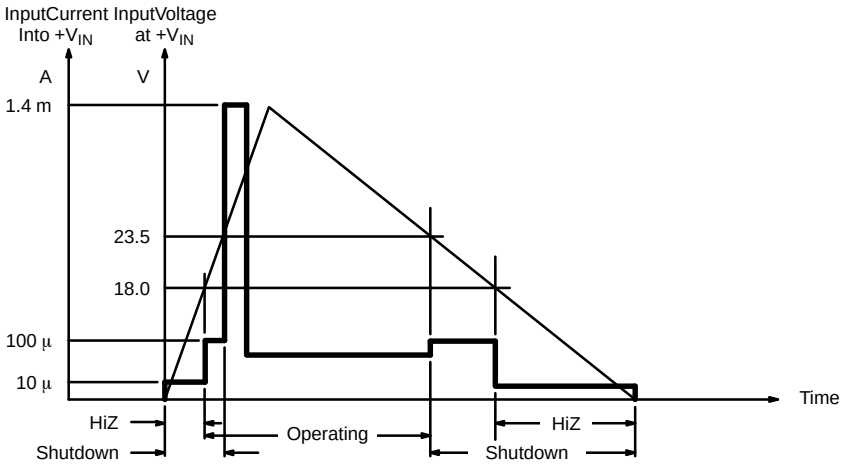



**FIGURE 1.** Input Current Behaviour

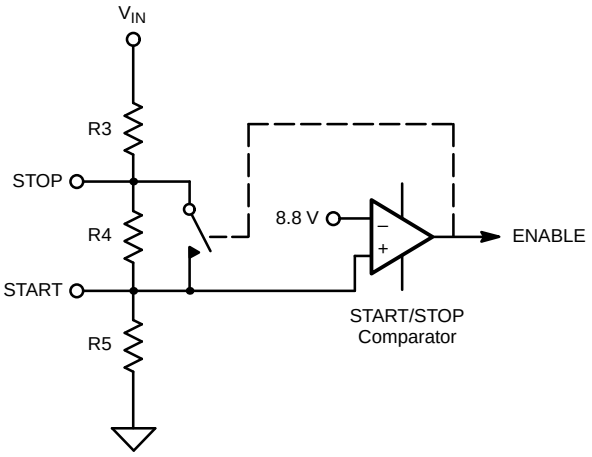



**FIGURE 2.** Start/Stop Programming

### Current Sense

The Si9113 has two integrated comparators. The PWM comparator, which is relatively slow, performs the current mode control function by comparing the output of the error amplifier with the current in the transformer primary. The overcurrent limit comparator is a faster channel from the current sense to the output driver and has a 100-ns typical propagation time.

With the current sense resistor in the primary path, a voltage signal which is proportional to the primary current is available to control the switch-on period. This signal is used by the PWM comparator as well as the overcurrent comparator. Selecting the right value and type of resistor is very important, as it determines the amount of power delivered to the load during fault conditions. At the same time, a higher resistor value can terminate the switching cycle prematurely and the circuit may not be able to deliver enough power to the load. Normally, it is recommended to derate the resistor by 20% of the value required to deliver the full power.

Taking this in account the $R_{SENSE}$ value shall be estimated by equation 3.

$$R_{SENSE} \leq \frac{0.2 \times V_{IN(min)} \times D_{MAX} \times \eta}{P_{OUT}} \quad (3)$$

where, $D_{MAX}$ = Maximum Duty Ratio
$P_{OUT}$ = Output Power (W)
$\eta$ = Converter Efficiency
$V_{IN(min)}$ = Minimum Input Voltage (V)

Ideally, when the flyback converter is in discontinuous mode, current rises at the rate determined by the input voltage and the primary inductance of the transformer (Figure 3). In the real world, however, a leading-edge spike is always created by the MOSFET gate and output capacitance, the interlayer capacitance of the primary and secondaries, the reverse recovery of their respective rectifiers, and the inductive nature of the current sense resistor. This leading edge spike may cause the switch to turn off prematurely unless it is filtered out by a low pass RC filter.

The leading edge spike includes a distinct component with a period equal to the fall time of the MOSFET drain along with the lower frequency oscillations. Obviously, it is difficult to estimate the amplitude and burst-width of these spikes. One easy approach is to measure on the oscilloscope, with a high sampling rate, the total width and amplitude of the burst under high-line and full-load conditions. Then design the RC network to integrate all these spikes in the burst. Usually, for the 20-kHz to 100-kHz converters, 200-ns to 50-ns time constants are a good compromise.

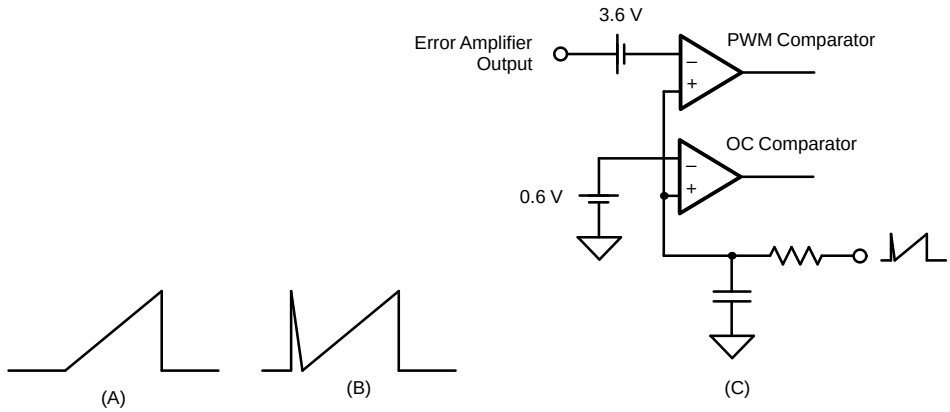



**FIGURE 3.** Low Pass RC Filter at Current Sense

**Compensation**

Compensating the loop at one particular line and load is not sufficient to ensure that the power supply will be equally stable under other line and load conditions. The loop can be compensated for all real-world conditions, but the margins will not be consistent.

The Si9113 is designed with a high open loop gain (up to 60 dB) and 1.3-MHz unity gain bandwidth. A fast inner control loop reduces propagation delays to achieve a good phase margin at high crossover frequencies. This reduces the compensation to the Type 2 network, where the low-frequency zero is introduced at the power stage low-frequency pole and the high-frequency pole is introduced at the output capacitor ESR zero. This high-frequency pole makes the compensation independent of the capacitor ESR and temperature, and also prevents thin high-frequency noise spikes from being amplified and transferred to the output.

Use the following guidelines to compensate the loop for the Si9113 multi-output converter:

Calculate the effective output filter capacity Ceff and the effective load resistor Reff of all the outputs at full load, reflected to the main output through the turns ratio. Use these values to locate the low-frequency power stage filter pole. (Refer to Figure 6)

$$C_{EFF} = C11 + \frac{NS2}{NS1} \times C10 + \left(\frac{NS1 + NS3}{NS1}\right) \times C4 = 246.6\ \mu F \quad (4)$$

For 800 mW of output power,

$$R_{EFF} = \frac{V_{3.3\,V}^{2}}{P_{OUT}} = 13.61\ \Omega \quad (5)$$

From equation 4 and 5, the power stage low-frequency pole is calculated as:

$$F_{PP} = \frac{1}{2\pi\, R_{EFF}\, C_{EFF}} = 47\ Hz \quad (6)$$

Calculate the power stage low-frequency gain. The low-frequency power stage gain is equal to the change in the power output per unit change in the error voltage, reflected by the change in peak primary current. Or keeping the $R_{EFF}$ the same, the change in the output voltage per unit change in the error amplifier output voltage. The energy transferred to the output during the off cycle is equal to the amount of energy stored in the transformer multiplied by the transformer and secondary circuit efficiency. The power input to the converter input is proportional to square of peak primary current (I-pk).

$$P_{IN} = \frac{1}{2}\, L_P (I_{PK})^2\, f_s$$
$$\frac{P_{OUT}}{\eta} = \frac{1}{2}\, L_P (I_{PK})^2\, f_s \quad (7)$$

or

$$I_{pk} = \sqrt{\frac{2\, P_{OUT}}{L_P \times f_s \times \eta}} = 192.45\ mA \quad (8)$$

With the current sensing resistor R7= 2 Ω, a 1-mV change in the error voltage will result in a 0.5-mA change in the peak primary current. All other parameters remaining same, the increase in the output power is:

$$P_O + \Delta P_O = \frac{1}{2}\, L_P (I_{PK} + \Delta I_{PK})^2 \times f_s \times \eta = 0.80416 \quad (9)$$

For a fixed effective impedance $R_{EFF}$,

$$V_O + \Delta V_O = \sqrt{(P_O + \Delta P_O) \times R_{EFF}} = 3.3083\ V \quad (10)$$

$$\text{The low frequency power stage gain} = 20\ \text{Log}\ \frac{\Delta V_O}{1\ mV} = 18.4\ dB \quad (11)$$

Plots of proposed close loop frequency response and power stage frequency response (Figure 4) suggest the nature of the error amplifier frequency response in terms of the location of low-frequency zero at $F_z$ and its gain at $F_z$.

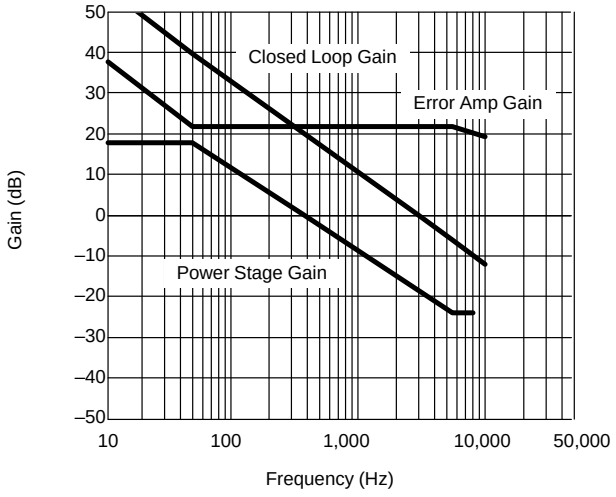



**FIGURE 4.** Calculated Loop Gain

The error amplifier low-frequency gain required from Figure 4 (ΔGain) = 23 dB.

$$R2 = R9 \times 10^{\frac{\Delta Gain}{20}} = 282\ k \quad \text{Use } 300\ k \tag{12}$$

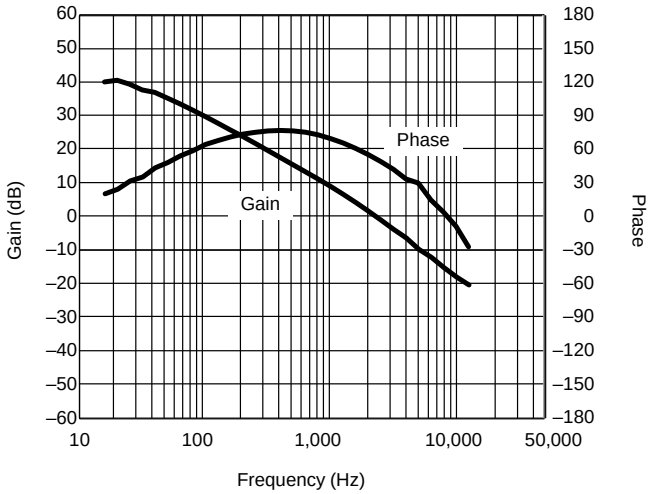



**FIGURE 5.** Measured Loop Gain

Introduce the error amplifier low–frequency zero at 47 Hz.

$$C8 = \frac{1}{2\pi \times f_z \times R2} = 0.011\ \mu F \quad \text{Use } 0.01\ \mu F \tag{13}$$

Normally, capacitor manufacturers quote the capacitor ESR values as maximums possible at a given frequency and temperature. The actual ESR figure is unknown and also varies with temperature. To make circuit stability independent of ESR zero, add a high frequency pole below the worst-case capacitor ESR zero location.

$$F_{p\_esr} = \frac{1}{2\pi\ R2\ C3} = \frac{1}{2\pi\ \times 300\ k \times 100\ pF} = 5.3\ kHz \tag{14}$$

Accounting for the phase lag, which results from the phase inversion, the output filter, the error amplifier pole at the origin and at the high frequency, and the phase lead resulting from the error amplifier zero the phase margin can be estimated.

$$\text{Phase Margin} = 90 - \tan^{-1}\frac{F_{CO}}{F_{p\_esr}} + \tan^{-1}\frac{F_{CO}}{F_z} - \tan^{-1}\frac{F_{CO}}{F_{pp}} \tag{15}$$

The same procedure should be repeated for 30% of the output power to make sure that the feedback loop is stable with enough margin. Figure 5 shows the actual closed loop gain and phase characteristics.

where, $C_{EFF}$ — Effective Output filter Capacity (F)
$R_{EFF}$ — Effictive Output Load Resistance (R)
$I_{PK}$ — Peak Primary Current (A)
$L_P$ — Transformer Primary Inductance (H)
$\eta$ — Converter Efficiency
$f_S$ — Switching Frequency (Hz)
$F_{PP}$ — Power Stage Low Frequency Pole (Hz)
$f_Z$ — Error Amp Low Frequency Zero (Hz)
$f_{co}$ — Close Loop Cross Over Frequency (Hz)
$f_{p\_esr}$ — Capacitor ESR Zero (Hz)

**Power Loss Consideration**

In the restricted power mode of TE, every milliwatt of power loss counts. Use the following guidelines to reduce the power loses to a minimum, especially at high line:

- Switching Frequency: The switching losses incurred in the transformer leakage inductance, the MOSFET gate, MOSFET drain voltage and current cross over, the output diode reverse recovery, and the control circuitry, are proportional to the switching frequency. The lowest possible operating frequency for a given form factor should be used to keep the switching losses to a minimum.

- Transformer: With an operating frequency range of 20 kHz, dc losses in the winding will usually be dominant. Leakage inductor spikes from charging the MOSFET output capacitor can also contribute to the losses, even though these are very low at lower switching frequencies. Select a core geometry and winding technique that achieves a good coupling between the primary and highest power output secondary. Refer to Vishay Siliconix application note AN713 for flyback transformer design guidelines.

- MOSFET switch: The dc and ac losses of the MOSFET switch should be balanced. The low gate charge and low gate-to-drain capacity MOSFET for a given $r_{DS(on)}$ should be selected to keep the gate charge loss and drain voltage and current cross over loss down. The Si3420DV, a 200-V LITTLE FOOT® TSOP-6 device, is the best choice for this application.

- Quiescent Current: The Si9113 uses a BiCMOS process to keep the control circuit operating current at low level. The power dissipated in the controller and MOSFET driver is equivalent to $V_{CC}$ multiplied by $I_{CC}$. Keep the worst-case low value of $V_{CC}$ just above the internal regulator voltage of 9.5 V. Also, make sure that the bootstrap voltage is always more than the maximum value of the internal regulator. Otherwise, more power will be dissipated in the internal depletion MOSFET.

- Other-Care should be taken to restrict the losses in the current and voltage sensing network, secondary rectifiers, and input and output capacitors. Refer to Vishay Siliconix application note AN704 for instructions on calculating power loss in the converter.

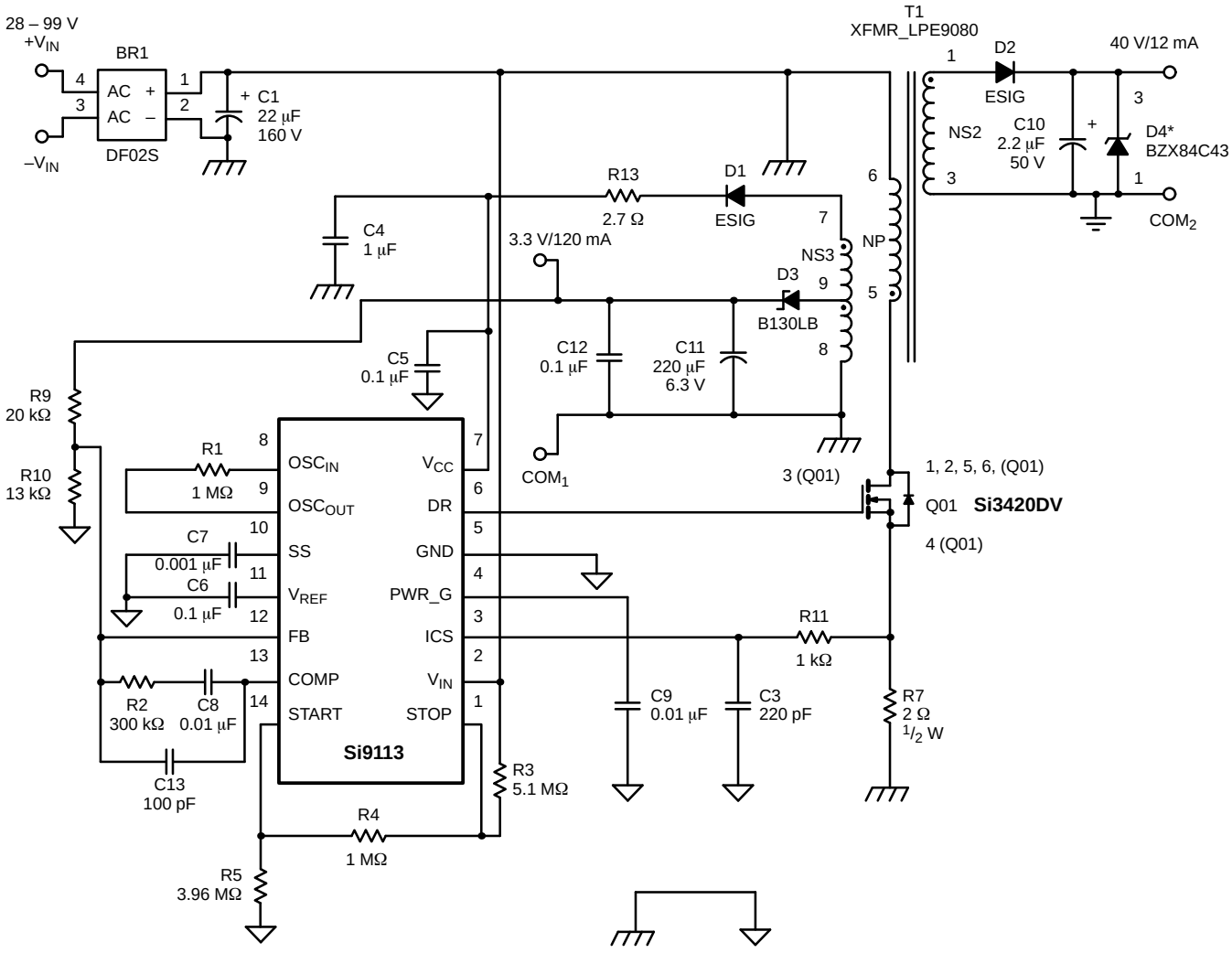



**FIGURE 6.** Dual Output Flyback converter with Tightly Regulated Main Output

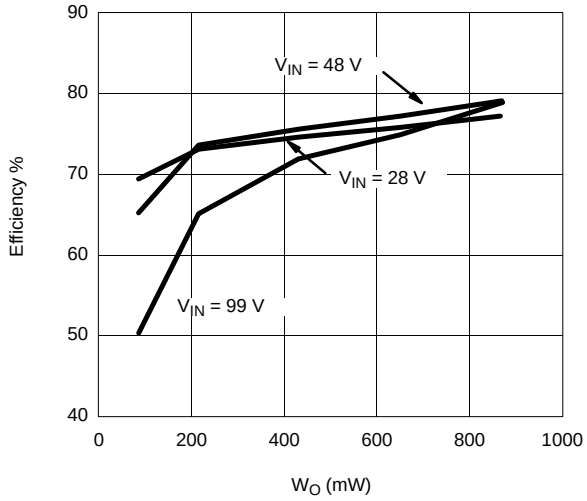
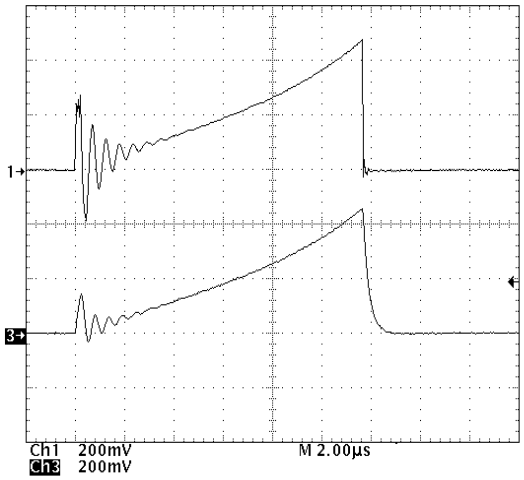
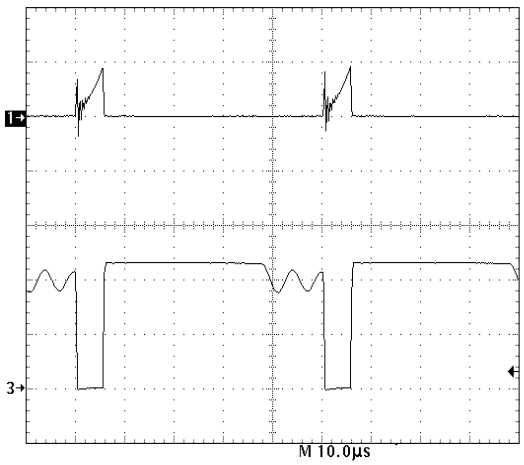



**FIGURE 7.** Efficiency vs. Output Power



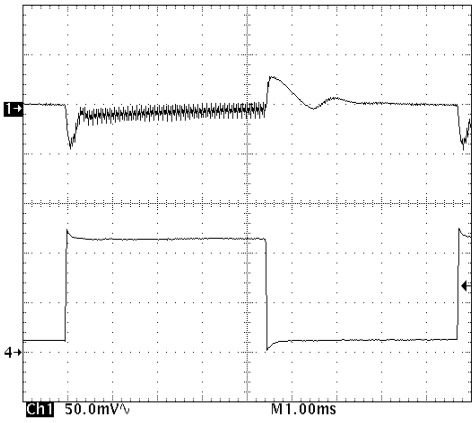

Ch1: Switch Current Before RC (0.1 A/div)
Ch3: Switch Current After RC (0.1 A/div)

**FIGURE 8.** Switch Current Waveform Before and After RC Network




$V_{IN}$ = 99 V
Output = 850 mW
Ch1: Switch Current (0.25 A/div)
Ch3: Drain Voltage (50 V/div)

**FIGURE 9.** Drain Switching Waveform




$V_{IN}$ = 48 V
$I_O$ @ 3.3 V = Step – 12 to 120 mA
$I_O$ @ 40 V = 12 mA
Ch1: $V_O$ = 3.3 V (50 mV/div)
Ch4: $I_O$ = 3.3 V (50 mA/div)

**FIGURE 10.** Transient Response—Main Output (3.3 V)

## ISDN CONCEPT

Integrated Services Digital Network (ISDN) is a combination of technology standards and regulations for digital telecommunications first proposed by the international telecommunications regulatory body, CCITT, in 1980. Intended to enable end-to-end digital communication of voice and data, the ISDN subscriber loop is key to the successful ISDN implementation because it must:

- Provide the user with a flexible digital interface with access to a wide variety of present and future services;
- Allow the evolution of the individual network services to progress towards achieving an ISDN according to the different strategies of the networks operators.

In analog transmission systems, the transmitted signals may represent analog or digital data. In either case, the signals are subject to attenuation, limiting the length of the transmission link. Even with repeaters, the signal-to-noise ratio still suffers over long distances. Digital signals, by contrast, are significantly more accurate.

Most of today's public switched telephone networks (PSTN) are digital, but the connection to end-customer telephone equipment—often called the subscriber loop—mostly employs analog techniques. The connection becomes dedicated for the duration of a call. For data terminals, packet switching is commonly used to support multiple logical connections and thus makes more efficient use of the connection bandwidth. Similar to the telephone network, the telex network also uses circuit switching but at a much slower speed. Consequently there is a tremendous pressure to integrate the series to achieve an efficient digital network.

As shown in Figure 11, the ISDN central office connects the numerous subscriber loops to the digital network. This provides access to a variety of lower OSI layers.

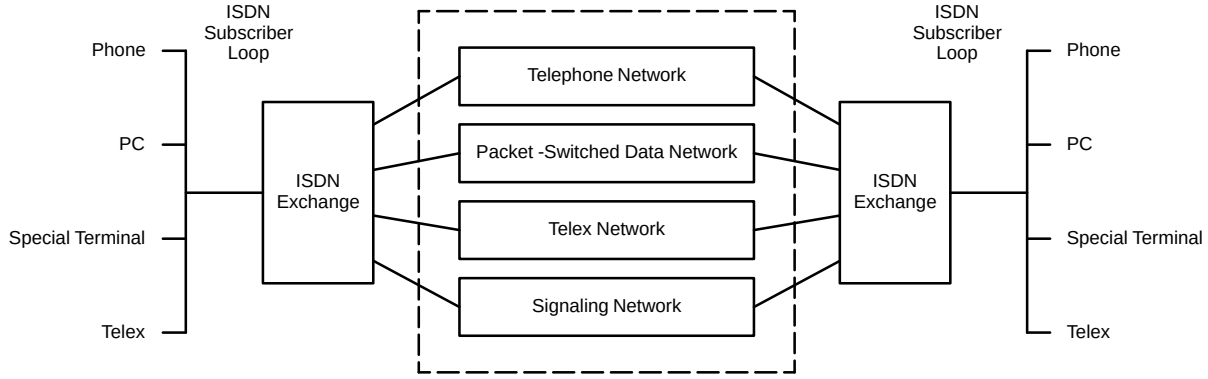



**FIGURE 11.** Integrated Digital Network

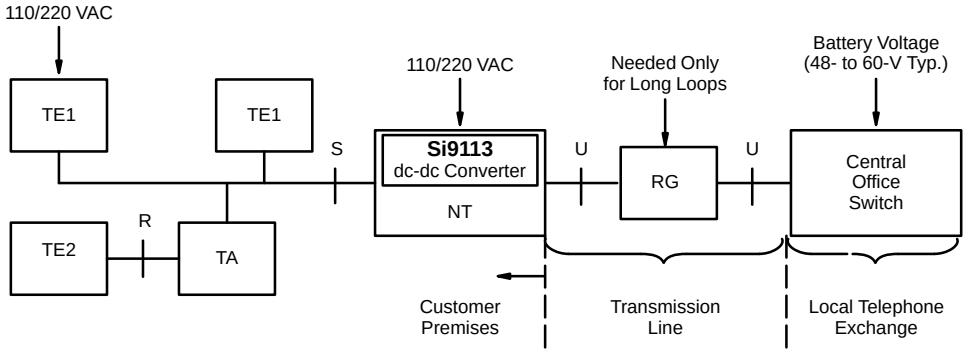



**FIGURE 12.** ISDN Functional Groups and Reference Points

## ISDN REFERENCE MODEL

Figure 12 is a reference model and shows how various functional groups are connected together to gain access to the ISDN network. The points which divide the functional groups are referred to as reference (interface) points, and will typically correspond to a particular physical interface connecting two pieces of equipment.

The S-interface is also known as the user-network interface (UNI) as it represents the common interface at which terminal equipment (TE) can be connected to the ISDN. The functions are:

- Terminal equipment, type 1 (TE1): examples are telephones, fax machines and videophones which can be directly connected to the S-interface and have the ability to establish and terminate a call.
- Terminal equipment, type 2 (TE2): examples are analog phones, computers, and communications terminal equipment. TE2's do not have an ISDN UNI and rely on a terminal adapter (TA) to operate as the TE1 functional group in order to connect to S-interface.
- Terminal adapter (TA): adapts a non-ISDN terminal to the ISDN. It will contain functions which include layer 1 (physical layer) and higher layers (including call processing) of the OSI reference model.
- Network Termination, type 1 (NT1): It marks the point at which the public network ends and the customer premise begins. NT1 equipment provides a conversion at the physical layer between S-interface that runs inside a customer premise and the subscriber loop cable at the U-interface that connects to the local exchange. An important function of NT1 is to feed power to the TE either from the local mains supply or from the network as a backup when the mains power fails.
- Network Termination, type 2 (NT2): Unlike NT1 equipment that provides only a physical translation between S- and U-interfaces, NT2 equipment may also incorporate more complex functions such as switching and multiplexing. A private branch exchange (PBX), inside customer premises, routes calls and provides its users with internal voice services, as well as access to external lines connected to the ISDN. Such an ISDN-based PBX belongs to the NT2.

Line Termination (LT): LT marks the end of the ISDN subscriber loop. It is typically located within the local exchange equipment as a line card containing the terminations for a number of subscriber lines. If the distance between LT and NT is greater than that supported by the U-interface, a signal regenerator (RG) is required.

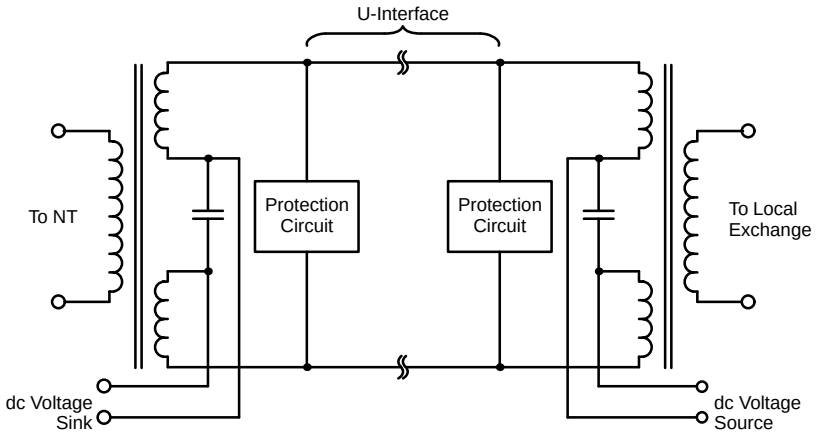



**FIGURE 13.** Power Feed Configuration at the U-Interface

## POWER FEEDING TO NT

Figure 13 illustrates the method used to provide a power feed across the U-interface from the local exchange to the NT1. The two conductors on the U-interface are separated with a capacitor to allow a dc voltage to be applied and to enable ac signals to pass without attenuation. Protection circuitry is added as needed.

Under normal conditions, the S-interface may be powered locally from the NT1 using mains or batteries, and is backed up with remote power from the network under emergency power conditions where the local power source fails.

When active, the NT1 must consume no more than 500 mW of power from the network, and in a deactivated state must consume no more than 120 mW. Under emergency power conditions when NT1 is expected to also power the user's designated TE across the S-interface, then the power consumption of an active NT1 is allowed to rise to a maximum of 1.1 W (although this varies between different ISDNs due to different safety requirements and subscriber loop configurations). The minimum voltage required for correct operation at the NT1 is 28 V, while the feed voltage at the exchange may vary among networks from 51 V to 115 V.

## POWER FEEDING TO TE

Power is fed from NT1 to TE in two configurations (Figure 14). In the first configuration, power source 1 (PS1) feeds power to the transformer at the NT, where the signal is injected. The signal is then recovered from the transformer at the TE. A dc-dc converter is used to power the TE circuitry.

In the second configuration, power source 2 (PS2) feeds power through a separate pair of conductors within the S-cable. These conductors are independent of the transmit and receive signal conductors. PS2 is capable of delivering higher levels of power to TEs. Power feeding designs and configurations vary among network operators and between different countries and regions.

Table 1 shows how a dc-dc converter feeds power to the S-interface on an NT1 board. Under normal conditions, the TE power comes from an ac-dc converter via a relay. In a mains failure condition, the relay switches the connection over to the dc-dc converter and polarity reverses. Such polarity reversal causes the TE to operate in restricted mode to minimize power drawn from U-interface.

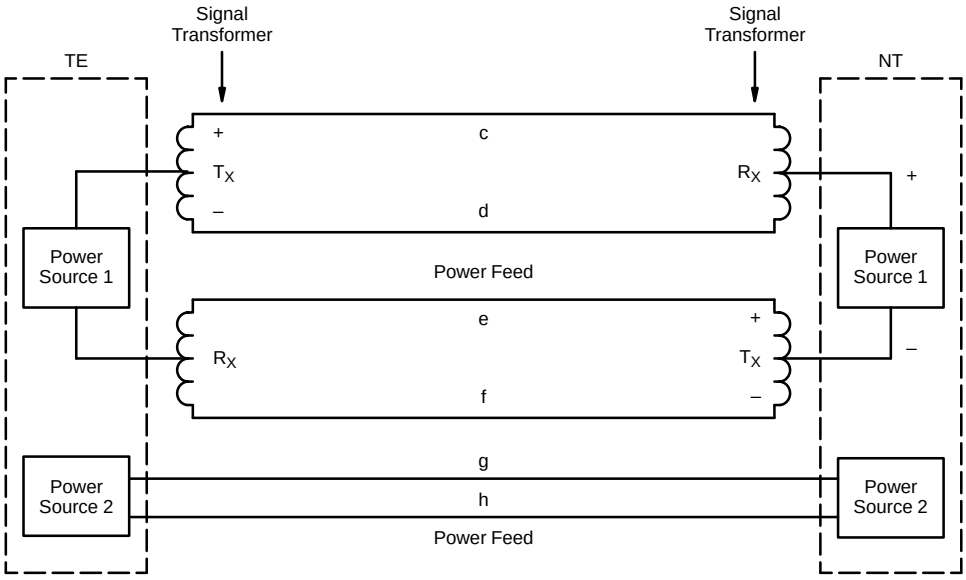



**FIGURE 14.** Power Feed Configurations at the S-Interface

## TE POWER STATES

Two states exist in which power is supplied to TE: normal and restricted. The state determines the maximum power levels supplied to TE by the power sources.

Under normal conditions, PS1 will deliver up to 1 W of power to an activated terminal on the S-interface. The restricted condition may be enforced under emergency conditions when the network or NT is forced to supply power in the event of a mains supply failure.

When supplying power via PS1, NT indicates this condition to TE by reversing the voltage polarity. This causes the attached TEs to enter a restricted mode of operation in which the designated TE can consume only 380 mW of power to remain operable. The power capabilities of PS1 and PS2 in normal and restricted modes are given in Table 1.

**TABLE 1 . POWER SOURCES SPECIFICATION**

| Condition | Power Source 1<br>ITU-T/ETSI, Nominal 40 V | Power Source 2<br>ITU-T/ETSI, Nominal 40 V |
|---|---|---|
| Voltage/Power at NT in Normal Mode | 34 to 42 V at up to max. power (1 W) | 42-V max. Min defined by TE requirements.<br>Max. power 8 W(ETSI-7 W) |
| Voltage/Power at NT in Restricted Mode | 34 to 42 V at up to 420 mW | 42-V max. Min defined by TE requirements.<br>Min. power 2 W |
| Voltage/Power at TE in Normal Mode | 24 to 42 V at up to 1 W | 32 to 42 V at min. power of 7 W |
| Voltage/Power at TE in Restricted Mode | 32 to 42 V at up to 401 mW. (380 mW for a designated at TE plus 21 mW for all other TEs combined) | 32 to 42 V at min. power of 2 W |

## BIBLIOGRAPHY

1. Nick Burd, The ISDN subscriber loop; Chapman & Hall
2. Power Integrated Circuit; Vishay Siliconix
3. Switching Power Supply Design; Abraham Pressman
4. G Dicenet, Design and prospects for the ISDN; Artech House
5. ETS 300 012-1 Integrated Services Digital Network (ISDN), Basic User Network Interface (UNI) Part 1: Layer 1 specification; ETSI
6. ETR 080 Transmission and Multiplexing (TM); Integrated Services Digital Network (ISDN) basic rate access; Digital transmission system on metallic local lines; ETSI