Dual Enhancement-Mode MOSFET (N- and P-Channel)

CHARACTERISTICS

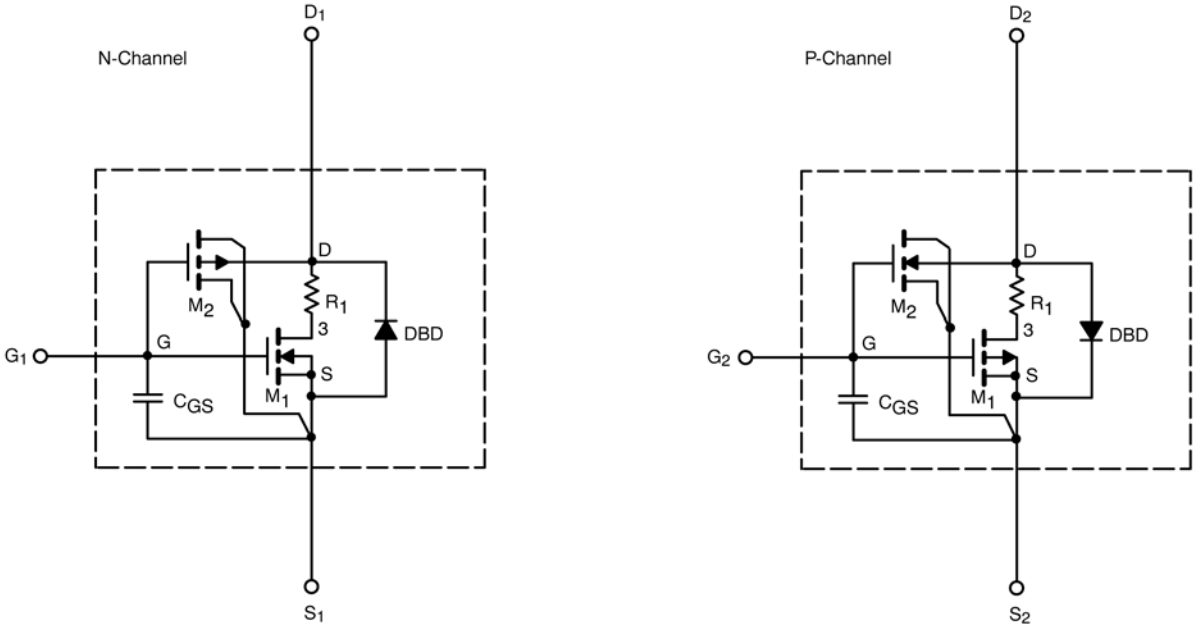
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



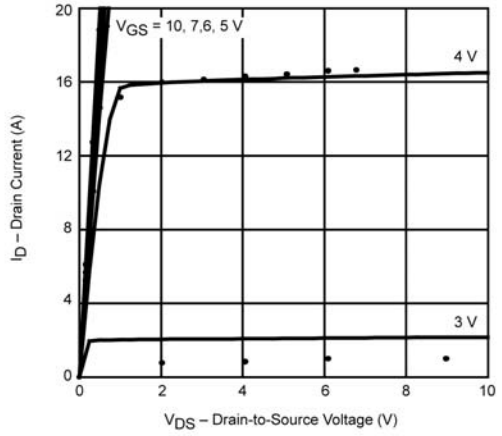
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

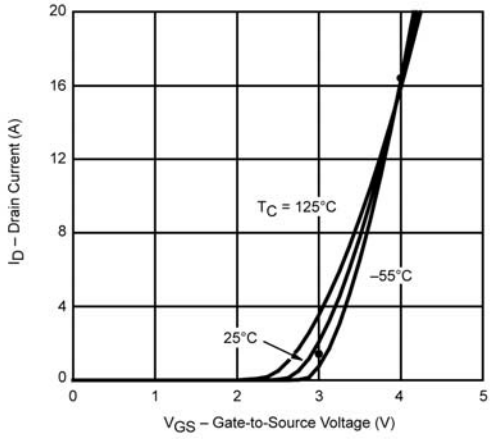
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	**Symbol**	**Test Condition**		**Typical**	**Unit**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V, V_{GS}, I_D = 250 μA	N-Ch	1.92	V
		V_{DS} = V, V_{GS}, I_D = –250 μA	P-Ch	2.13	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	N-Ch	176	A
		$V_{DS} \geq$ –5 V, V_{GS} = –10 V	P-Ch	132	
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 4 A	N-Ch	0.026	Ω
		V_{GS} = –10 V, I_D = 3.5 A	P-Ch	0.034	
		V_{GS} = 4.5 V, I_D = 3.4 A	N-Ch	0.037	
		V_{GS} = –4.5 V, I_D = 2.5 A	P-Ch	0.054	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 4 A	N-Ch	11	S
		V_{DS} = –15 V, I_D = –3.5 A	P-Ch	9.6	
Diode Forward Voltage[a]	V_{SD}	I_S = 1.25 A, V_{GS} = 0 V	N-Ch	0.76	V
		I_S = –1.25 V, V_{GS} = 0 V	P-Ch	–0.78	
Dynamic[b]					
Total Gate Charge	Q_g	N-Channel V_{DS} = 15 V, V_{GS} = 10 V, I_D = 4 A P-Channel V_{DS} = –15 V, V_{GS} = –10 V, I_D = –3.5 A	N-Ch	17.5	nC
			P-Ch	18	
Gate-Source Charge	Q_{gs}		N-Ch	4	
			P-Ch	4.4	
Gate-Drain Charge	Q_{gd}		N-Ch	2.5	
			P-Ch	3.1	
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} =15 V, R_L = 15 Ω $I_D \cong$ 1 A, V_{GEN} = 10 V, R_G = 6 Ω P-Channel V_{DD} = –15 V, R_L = 15 Ω $I_D \cong$ –1 A, V_{GEN} = –10 V, R_G = 6 Ω	N-Ch	14	ns
			P-Ch	14	
Rise Time	t_r		N-Ch	6.2	
			P-Ch	7.8	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch	23.6	
			P-Ch	21	
Fall Time	t_f		N-Ch	11	
			P-Ch	11	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.25A, di/dt = 100 A/μs	N-Ch	25.8	
			P-Ch	30	

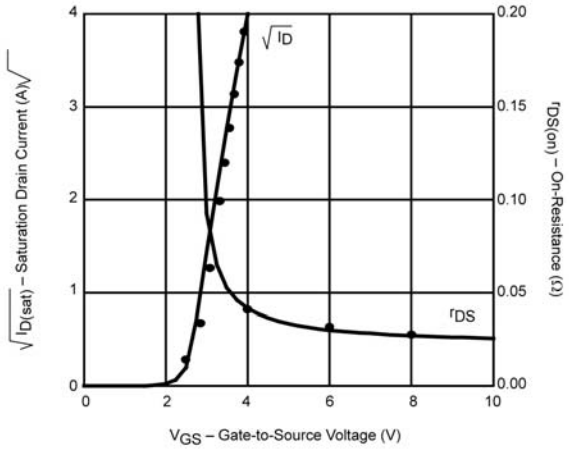
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

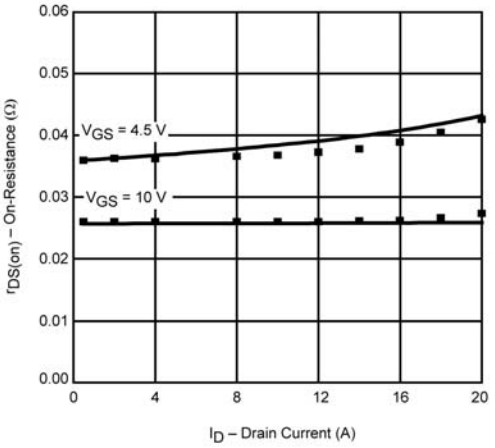
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

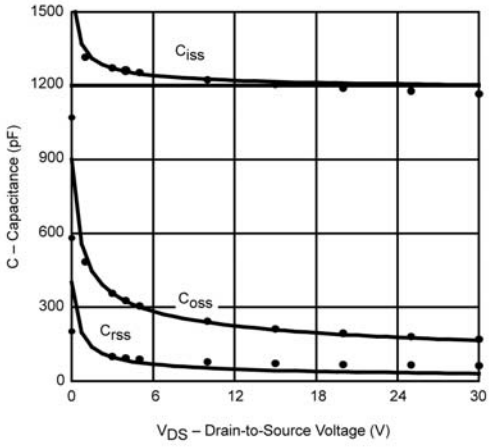
N-Channel MOSFET

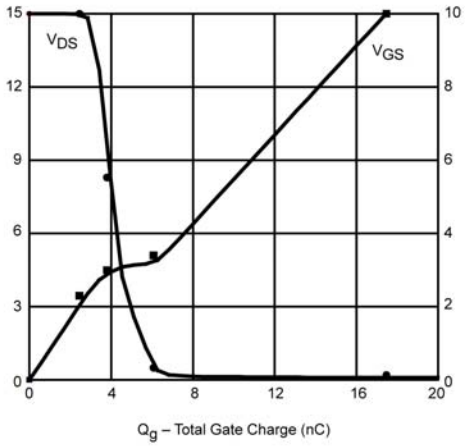






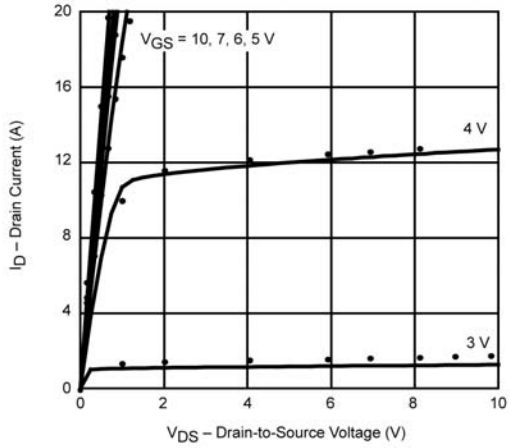


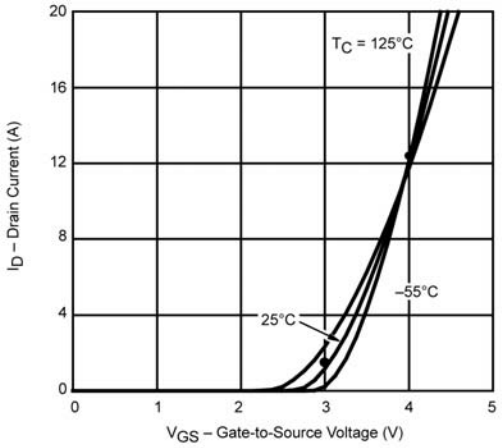


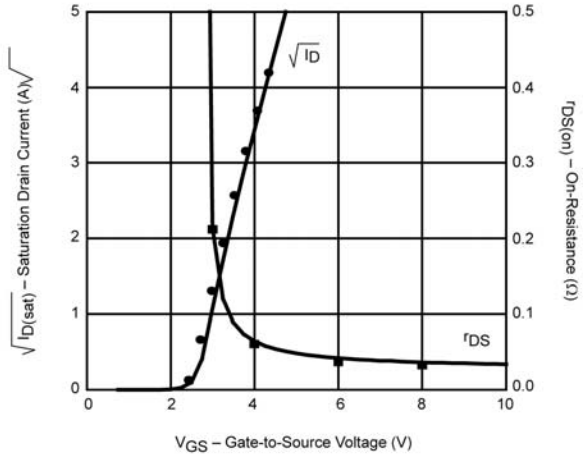


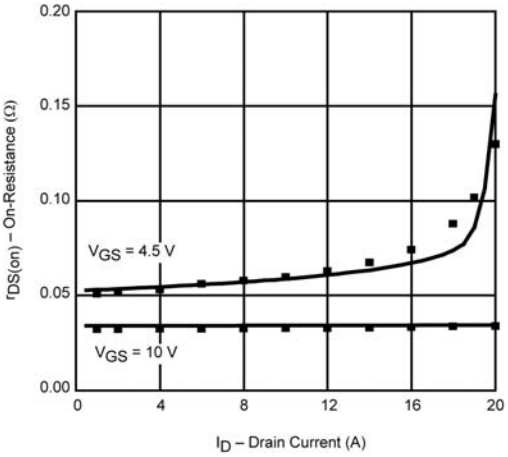
Note: Dots and squares represent measured data.

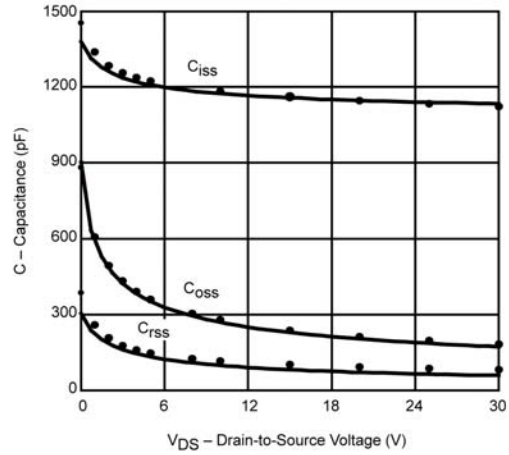
P-Channel MOSFET

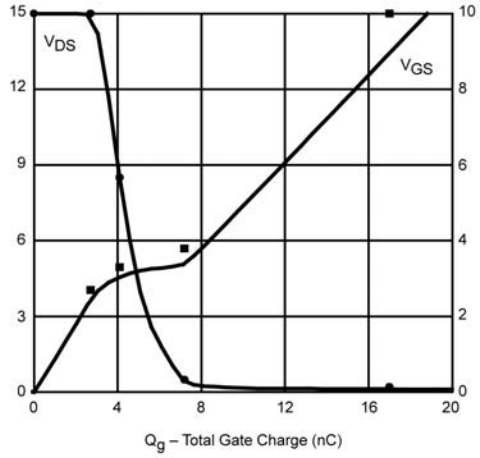












Note: Dots and squares represent measured data.

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