



Dual N- and P-Channel 2.5-V (G-S) MOSFET

CHARACTERISTICS

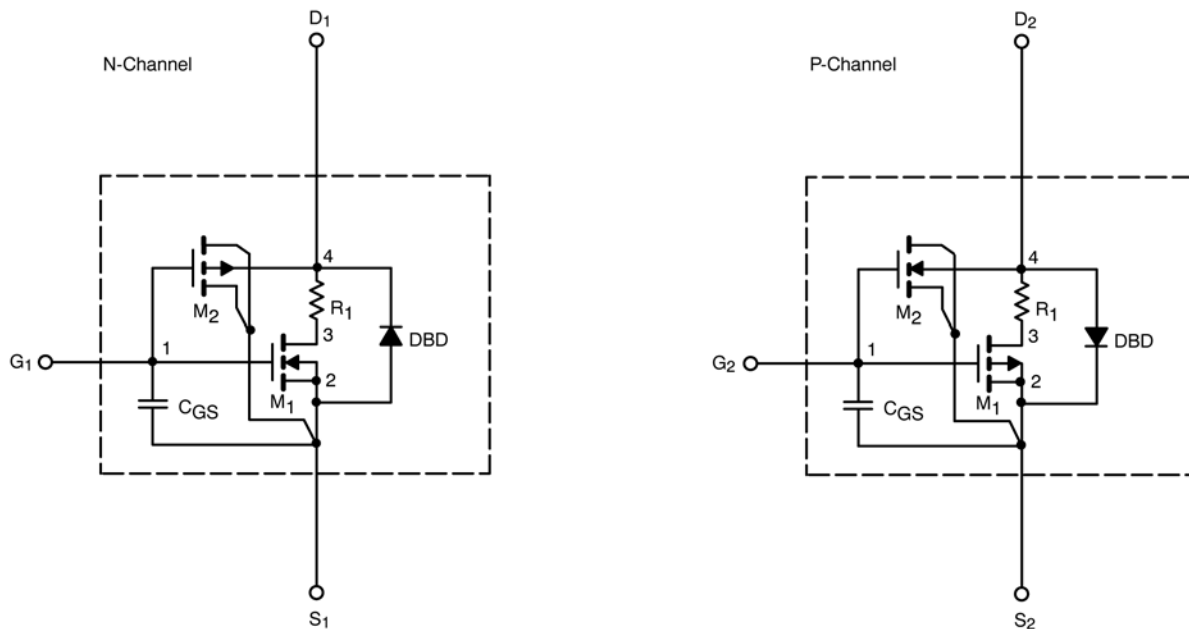
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Typical	Unit		
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V, V _{GS} , I _D = 250 μA	N-Ch	0.93	V	
		V _{DS} = V, V _{GS} , I _D = -250 μA	P-Ch	1.01		
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	N-Ch	152	A	
		V _{DS} ≤ -5 V, V _{GS} = -4.5 V	P-Ch	90		
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 7.1 A	N-Ch	0.019	Ω	
		V _{GS} = -4.5 V, I _D = -6.2 A	P-Ch	0.030		
		V _{GS} = 2.5 V, I _D = 6 A	N-Ch	0.024		
		V _{GS} = -2.5 V, I _D = -5 A	P-Ch	0.043		
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 7.1 A	N-Ch	28	S	
		V _{DS} = -10 V, I _D = -6.2 A	P-Ch	16		
Diode Forward Voltage ^a	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V	N-Ch	0.72	V	
		I _S = -1.7 V, V _{GS} = 0 V	P-Ch	-0.75		
Dynamic^b						
Total Gate Charge ^b	Q _g	N-Channel V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 7.1 A P-Channel V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -6.2 A	N-Ch	21	nC	
Gate-Source Charge ^b	Q _{gs}		P-Ch	22		
			N-Ch	6.5		
Gate-Drain Charge ^b	Q _{gd}		P-Ch	7		
			N-Ch	4		
			P-Ch	3.5		
Turn-On Delay Time ^b	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _G = 6 Ω P-Channel V _{DD} = -10 V, R _L = 10 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω	N-Ch	36	ns	
			P-Ch	15		
Rise Time ^b	t _r		N-Ch	37		
			P-Ch	29		
Turn-Off Delay Time ^b	t _{d(off)}		N-Ch	78		
			P-Ch	95		
Fall Time ^b	t _f		N-Ch	33		
			P-Ch	25		
Source-Drain Reverse Recovery Time	t _{rr}		I _F = 1.7 A, di/dt = 100 A/μs	N-Ch		43
			I _F = -1.7 A, di/dt = 100 A/μs	P-Ch		46

Notes

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

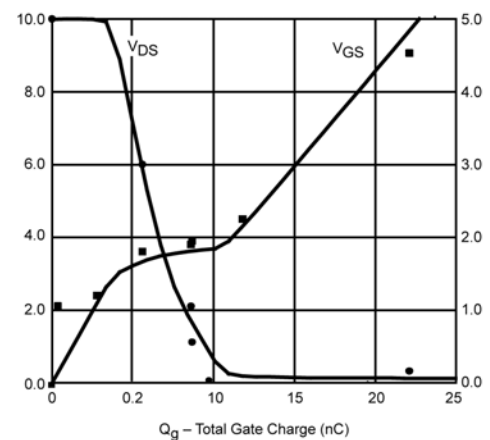
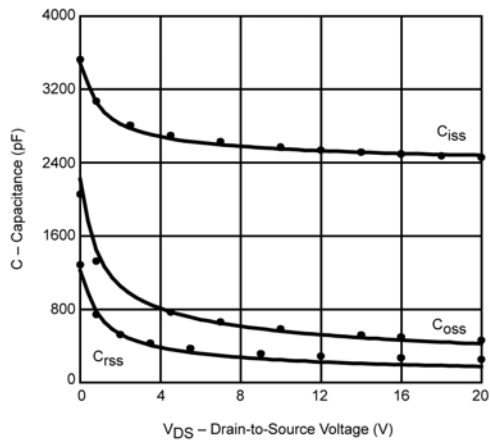
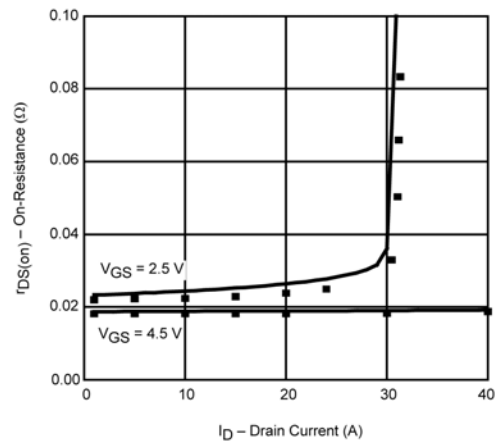
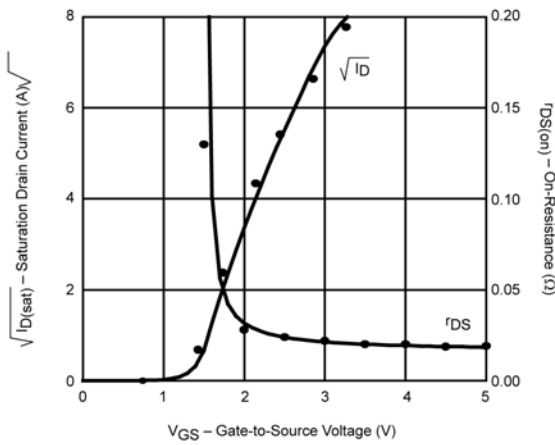
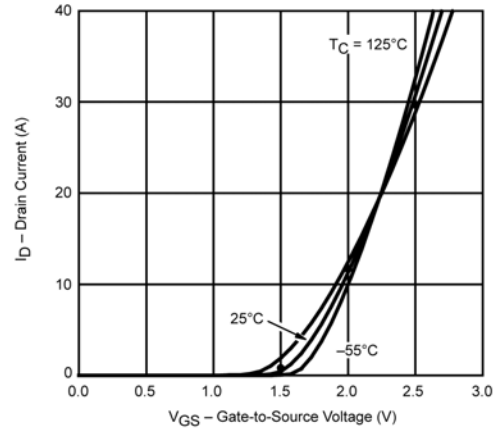
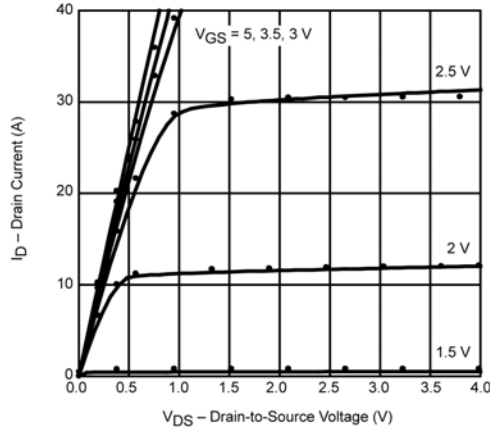


SPICE Device Model Si4562DY

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COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

N-Channel MOSFET



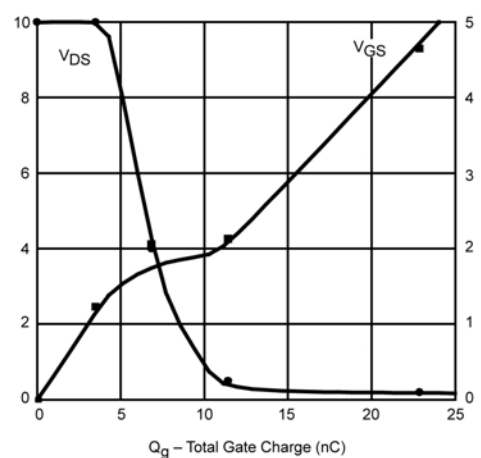
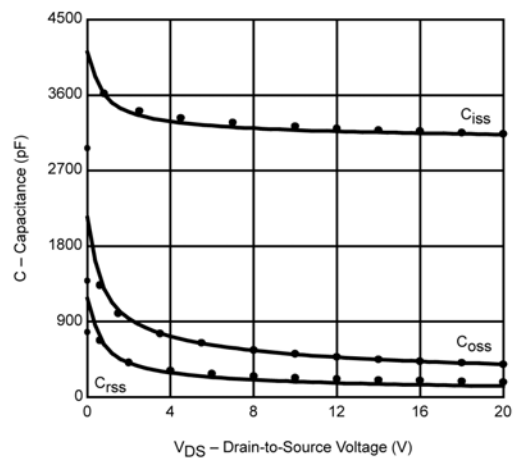
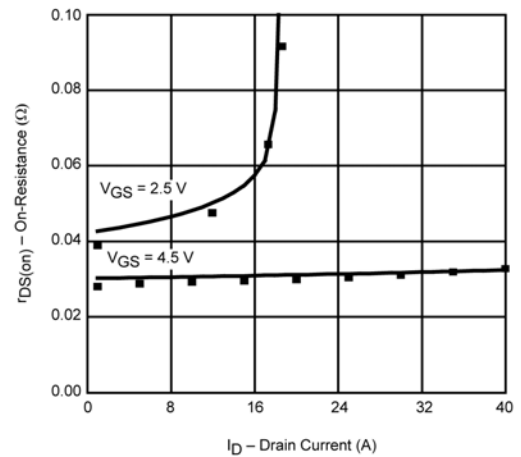
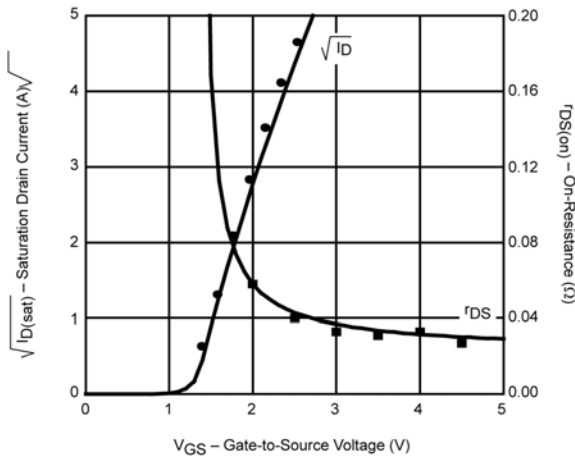
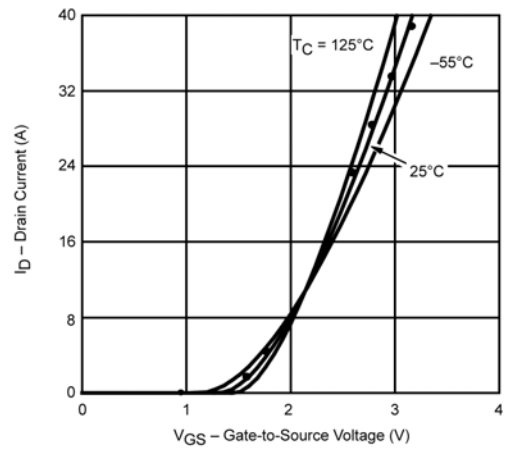
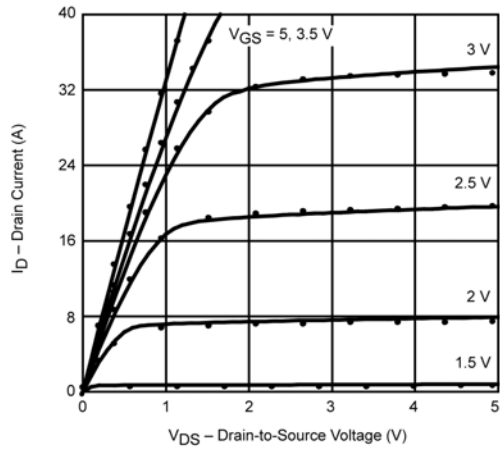
Note: Dots and squares represent measured data.

SPICE Device Model Si4562DY

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P-Channel MOSFET



Note: Dots and squares represent measured data.



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