



Complementary 20-V (D-S) MOSFET

CHARACTERISTICS

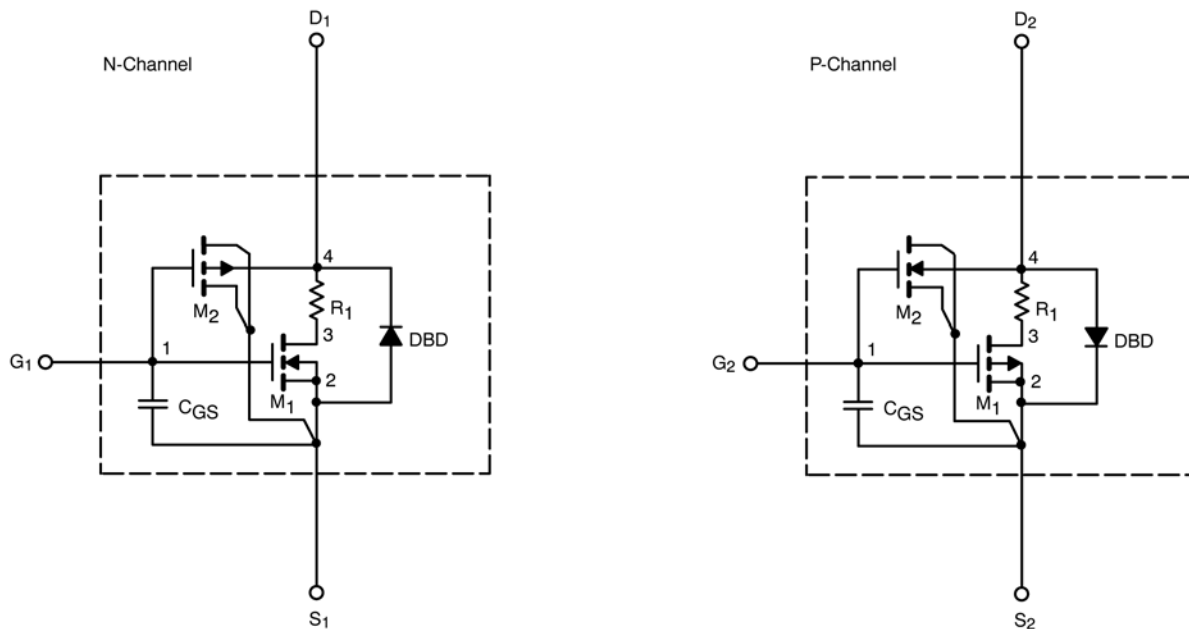
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Typical	Unit	
Static					
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V, V _{GS} , I _D = 250 μA	N-Ch	1.02	V
		V _{DS} = V, V _{GS} , I _D = -250 μA	P-Ch	1.02	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	N-Ch	32	A
		V _{DS} ≤ -5 V, V _{GS} = -4.5 V	P-Ch	20	
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 3.1 A	N-Ch	0.0065	Ω
		V _{GS} = -4.5 V, I _D = -2.1 A	P-Ch	0.133	
		V _{GS} = 2.5 V, I _D = 2.3 A	N-Ch	0.110	
		V _{GS} = -2.5 V, I _D = -1.7 A	P-Ch	0.216	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 3.1 A	N-Ch	7	S
		V _{DS} = -10 V, I _D = -2.1 A	P-Ch	5	
Diode Forward Voltage ^a	V _{SD}	I _S = 0.9 A, V _{GS} = 0 V	N-Ch	0.80	V
		I _S = -0.9 A, V _{GS} = 0 V	P-Ch	-0.80	
Dynamic^b					
Total Gate Charge	Q _g	N-Channel V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 3.1 A P-Channel V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -2.1 A	N-Ch	3.2	nC
Gate-Source Charge	Q _{gs}		P-Ch	3	
			N-Ch	0.60	
Gate-Drain Charge	Q _{gd}		P-Ch	0.90	
			N-Ch	1.3	
Turn-On Delay Time	t _{d(on)}		P-Ch	0.60	
		N-Ch	11	ns	
Rise Time	t _r	P-Ch	16		
		N-Ch	14		
Turn-Off Delay Time	t _{d(off)}	P-Ch	19		
		N-Ch	16		
Fall Time	t _f	P-Ch	22		
		N-Ch	20		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 0.9 A, di/dt = 100 A/μs	N-Ch		40
		I _F = -0.9 A, di/dt = 100 A/μs	P-Ch	36	

Notes

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

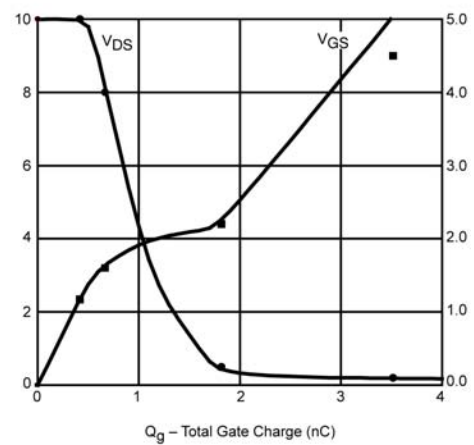
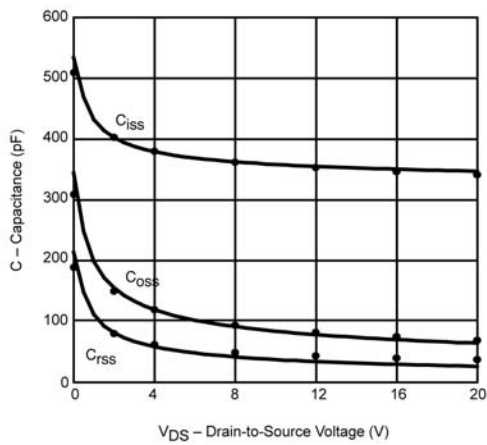
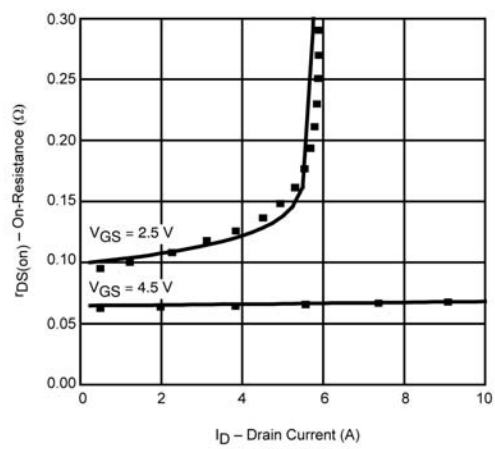
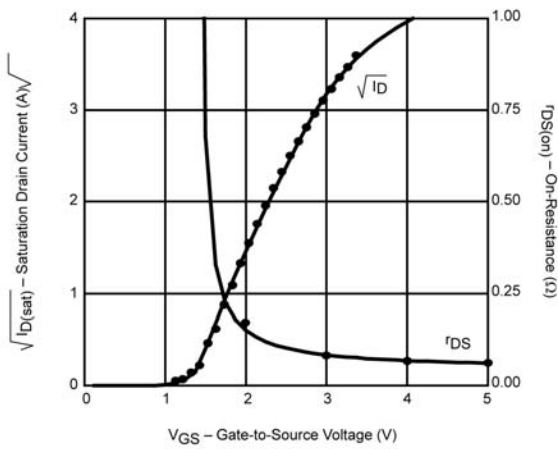
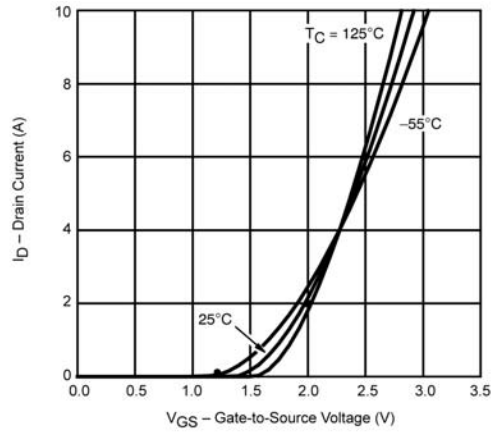
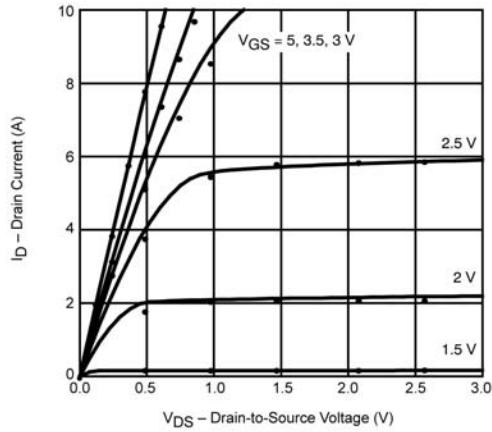


SPICE Device Model Si5513DC

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COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

N-Channel MOSFET



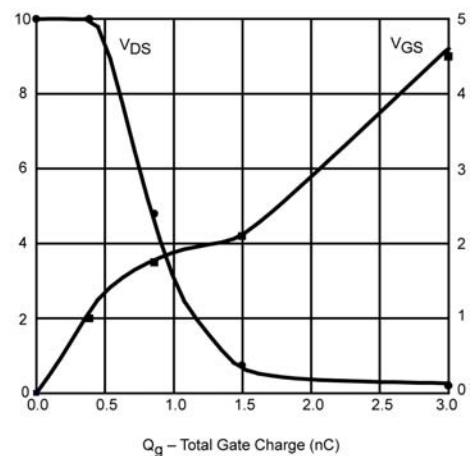
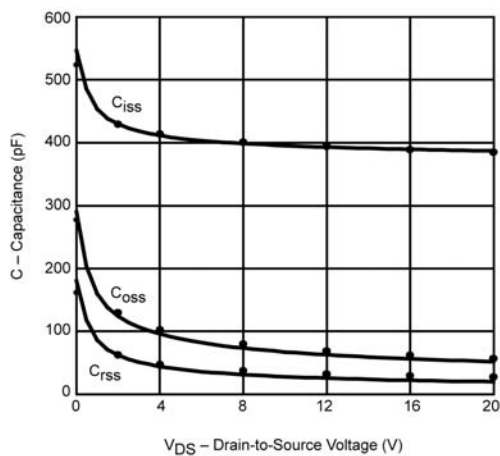
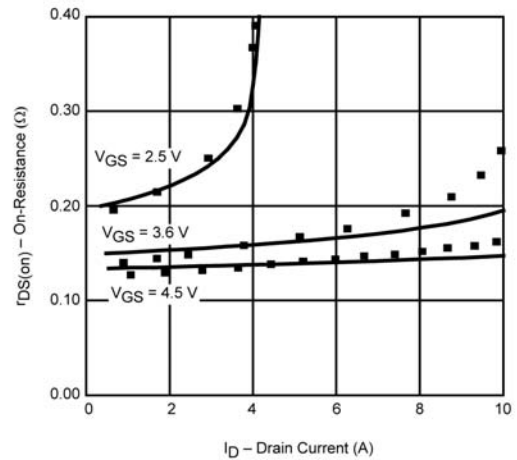
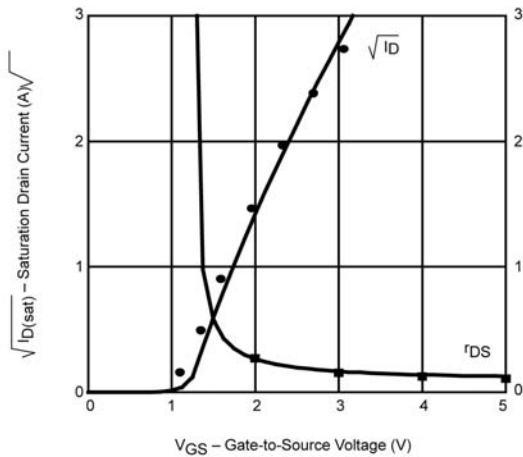
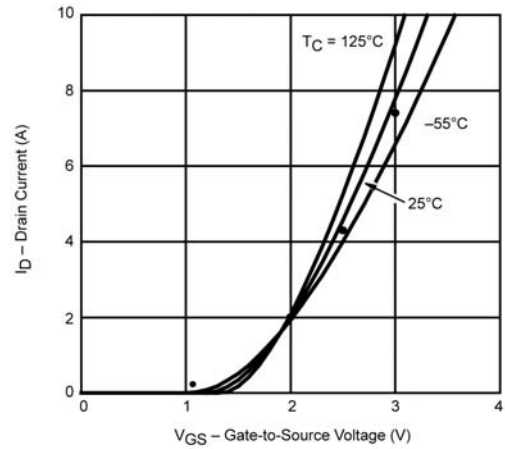
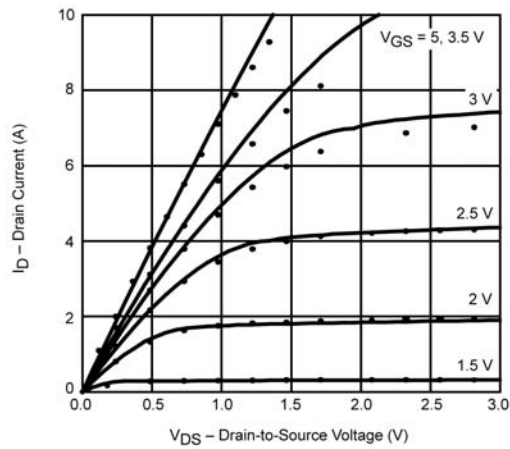
Note: Dots and squares represent measured data.

SPICE Device Model Si5513DC

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P-Channel MOSFET



Note: Dots and squares represent measured data.



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