Low-Voltage Single Asymmetrical SPDT Analog Switch

DESCRIPTION

The DG2020 is a single-pole/double-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed, low on-resistance and small physical size, the DG2020 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG2020 is built on Vishay Siliconix's low voltage JI2 process. An epitaxial layer prevents latchup. Break-before-make is guaranteed.

The switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FEATURES

- Low voltage operation (2.7 V to 5.5 V)
- Low on-resistance - R_{ON}
  - NO = 0.8 Ω
  - NC = 1.2 Ω
- Low power consumption
- TTL/CMOS compatible
- TSOP-6 package

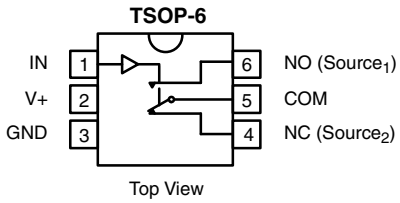
BENEFITS

- Reduced power consumption
- Simple logic interface
- High accuracy
- Reduce board space

APPLICATIONS

- Cellular phones
- Communication systems
- Portable test equipment
- Battery operated systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device Marking: E3xxx

TRUTH TABLE		
LOGIC	NC	NO
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
TEMP. RANGE	PACKAGE	PART NUMBER
- 40 °C to 85 °C	TSOP-6	DG2020DV

ABSOLUTE MAXIMUM RATINGS			
PARAMETERS	CONDITIONS	LIMITS	UNIT
V+	Reference to GND	- 0.3 to 6	V
IN, COM, NC, NO[a]	Reference to GND	- 0.3 to (V+ + 0.3 V)	
Continuous Current (any terminal)	Reference to GND	± 50	mA
Peak Current (pulsed at 1 ms, 10 % duty cycle)	Reference to GND	± 200	
Storage Temperature (D suffix)	Reference to GND	- 65 to + 125	°C
TSOP-6[c]	Power Dissipation (packages)[b]	570	mW

Notes

a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 7 mW/C above 25 °C.

SPECIFICATION (V+ = 3 V)							
PARAMETER	SYMBOL	TEST CONDITION UNLESS OTHERWISE SPECIFIED, V+ = 3 V, ± 10 %, V_{IN} = 0.4 V or 2 V[e]	TEMP.[a]	LIMITS (- 40 °C TO 85 °C) MIN.[b]	TYP.[c]	MAX.[b]	UNIT
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0	-	V+	V
On-Resistance	$R_{ON(NO)}$	V+ = 2.7 V, V_{COM} = 1.5 V, I_{NO}, I_{NC} = 100 mA	Room	-	1.4	2	Ω
			Full	-	1.5	2.1	
	$R_{ON(NC)}$		Room	-	2.2	3.2	
			Full	-	2.3	3.3	
R_{ON} Flatness[d]	$R_{ON(NO)}$ Flatness	V+ = 2.7 V, V_{COM} = 0 V to V+, I_{NO}, I_{NC} = 100 mA	Room	-	0.42	-	
Switch Off Leakage Current[f]	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 3.3 V, V_{NO}, V_{NC} = 1 V/3 V, V_{COM} = 3 V/1 V	Room	- 2.3	-	2.3	nA
			Full	- 60	-	60	
	$I_{COM (off)}$		Room	- 2.3	-	2.3	
			Full	- 60	-	60	
Channel-On Leakage Current[f]	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 1 V/3 V	Room	- 2.3	-	2.3	
			Full	- 60	-	60	
Digital Control							
Input High Voltage	V_{INH}		Full	2	-	-	V
Input Low Voltage	V_{INL}		Full	-	-	0.4	
Input Capacitance	C_{IN}		Full	-	3.7	-	pF
Input Current	I_{NL} or I_{NH}	V_{IN} = 0 or V+	Full	1	-	1	µA
Dynamic Characteristics							
Turn-On Time	$t_{ON(NO)}$	V_{NO} or V_{NC} = 2 V, R_L = 300 Ω, C_L = 35 pF	Room	-	6	10	µs
			Full	-	-	11	
	$t_{ON(NC)}$		Room	-	5	7	
			Full	-	-	8	
Turn-Off Time	$t_{OFF(NO)}$		Room	-	2	5	
			Full	-	-	5.5	
	$t_{OFF(NC)}$		Room	-	2	4	
			Full	-	-	4.5	
Break-Before-Make Time	t_d	V_{NO} or V_{NC} = 2 V, R_L = 300 Ω, C_L = 35 pF	Full	1	3	-	
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room	-	1	-	pC
Off-Isolation[d]	QIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	- 52	-	dB
Crosstalk[d]	X_{TALK}		Room	-	- 53	-	
NO, NC Off Capacitance[d]	$t_{ON(NO)}$	V_{IN} = 0 or V+, f = 1 MHz	Room	-	75	-	pF
	$t_{ON(NC)}$		Room	-	34	-	
Channel-On Capacitance[d]	$t_{OFF(NO)}$		Room	-	88	-	
	$t_{OFF(NC)}$		Room	-	95	-	
Power Supply							
Power Supply Range	V+		-	2.7	-	3.3	V
Power Supply Current	I+	V_{IN} = 0 or V+	Full	-	0.2	1	µA
Power Consumption	P_C		Full	-	-	3.3	µW

Notes

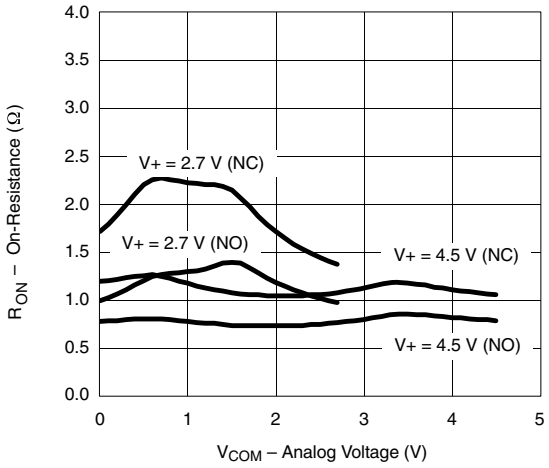
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 5 V leakage testing, not production tested.

SPECIFICATION (V+ = 5 V)							
PARAMETER	SYMBOL	TEST CONDITION UNLESS OTHERWISE SPECIFIED, V+ = 5 V, ± 10 %, V_{IN} = 0.8 V or 2.4 V[e]	TEMP.[a]	LIMITS (- 40 °C TO 85 °C) MIN.[b]	TYP.[c]	MAX.[b]	UNIT
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0	-	V+	V
On-Resistance	$R_{ON(NO)}$	V+ = 4.5 V, V_{COM} = 3 V, I_{NO}, I_{NC} = 100 mA	Room	-	0.8	1.1	Ω
			Full	-	0.9	1.2	
	$R_{ON(NC)}$		Room	-	1.2	1.6	
			Full	-	1.3	1.7	
R_{ON} Flatness[d]	$R_{ON(NO)}$ Flatness	V+ = 4.5 V, V_{COM} = 0 V to V+, I_{NO}, I_{NC} = 100 mA	Room	-	0.13	-	
Switch Off Leakage Current	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 5.5 V, V_{NO}, V_{NC} = 1 V/4.5 V, V_{COM} = 4.5 V/1 V	Room	- 5.3	-	5.3	nA
			Full	- 98	-	98	
	$I_{COM (off)}$		Room	- 5.3	-	5.3	
			Full	- 98	-	98	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 5.5 V, V_{NO}, V_{NC} = V_{COM} = 1 V/4.5 V	Room	- 5.3	-	5.3	
			Full	- 98	-	98	
Digital Control							
Input High Voltage	V_{INH}		Full	2.4	-	-	V
Input Low Voltage	V_{INL}		Full	-	-	0.8	
Input Capacitance	C_{IN}		Full	-	3.5	-	pF
Input Current	I_{NL} or I_{NH}	V_{IN} = 0 or V+	Full	1	-	1	µA
Dynamic Characteristics							
Turn-On Time	$t_{ON(NO)}$	V_{NO} or V_{NC} = 3 V, R_L = 300 Ω, C_L = 35 pF	Room	-	3	6	µs
			Full	-	-	6.5	
	$t_{ON(NC)}$		Room	-	2	5	
			Full	-	-	5.5	
Turn-Off Time	$t_{OFF(NO)}$		Room	-	1	4	
			Full	-	-	4.5	
	$t_{OFF(NC)}$		Room	-	1	3	
			Full	-	-	3.5	
Break-Before-Make Time	t_d	V_{NO} or V_{NC} = 3 V, R_L = 300 Ω, C_L = 35 pF	Full	0.3	1.5	-	
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room	-	5	-	pC
Off-Isolation[d]	QIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	- 53	-	dB
Crosstalk[d]	X_{TALK}		Room	-	- 54	-	
NO, NC Off Capacitance[d]	$t_{ON(NO)}$	V_{IN} = 0 or V+, f = 1 MHz	Room	-	65	-	pF
	$t_{ON(NC)}$		Room	-	32	-	
Channel-On Capacitance[d]	$t_{OFF(NO)}$		Room	-	90	-	
	$t_{OFF(NC)}$		Room	-	95	-	
Power Supply							
Power Supply Range	V+			4.5	-	5.5	V
Power Supply Current	I+	V_{IN} = 0 or V+	Full	-	0.2	1	µA
Power Consumption	P_C		Full	-	-	5.5	µW

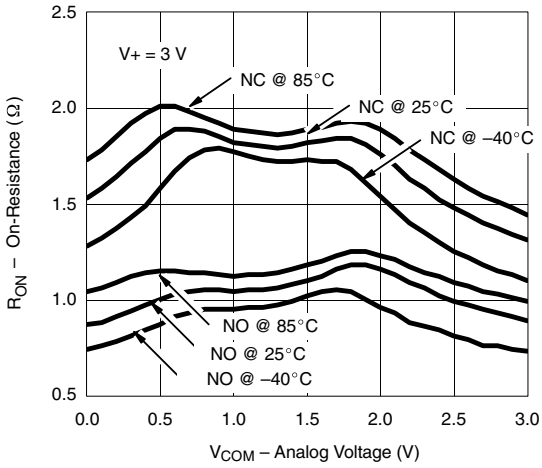
Notes

a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 5 V leakage testing, not production tested..

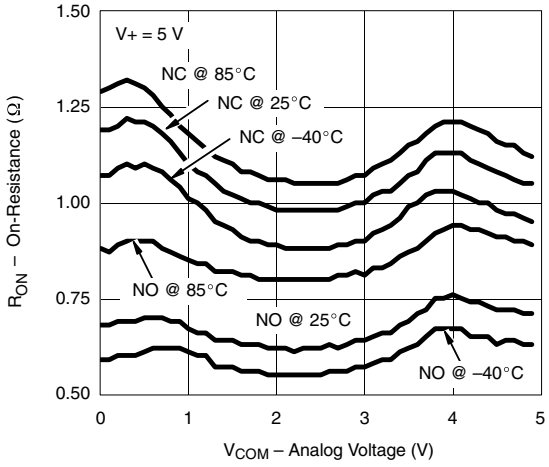
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



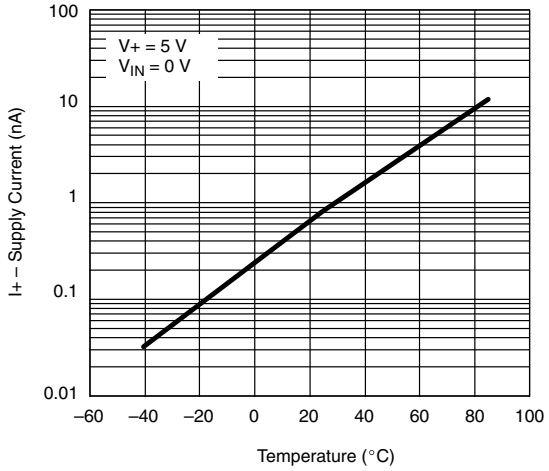
R_{ON} vs. V_{COM} and Supply Voltage



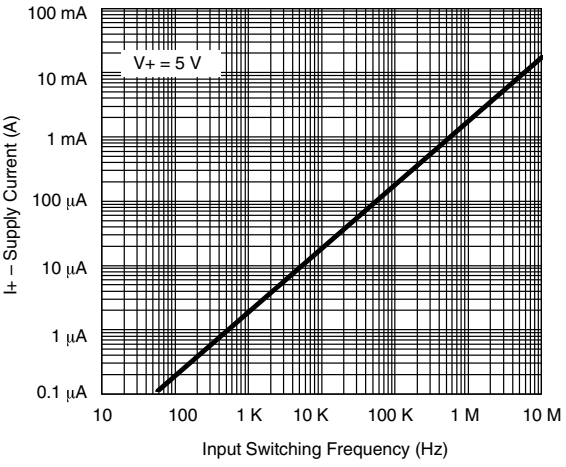
R_{ON} vs. Analog Voltage and Temperature



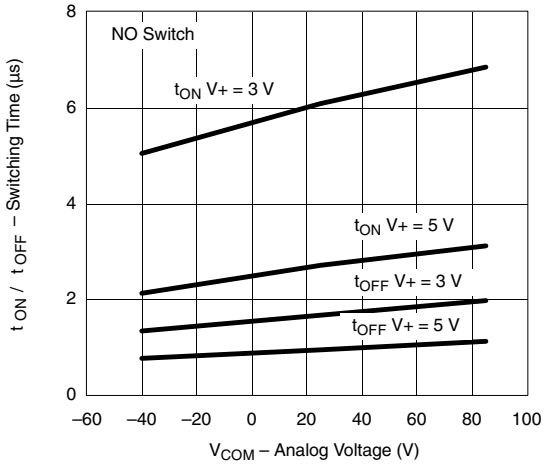
R_{ON} vs. Analog Voltage and Temperature



Supply Current vs. Temperature

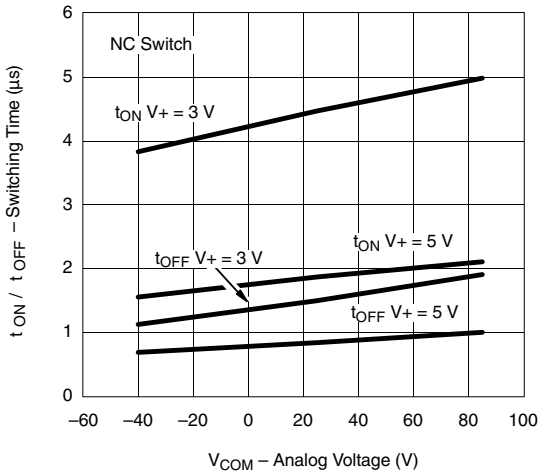


Supply Current vs. Input Switching Frequency

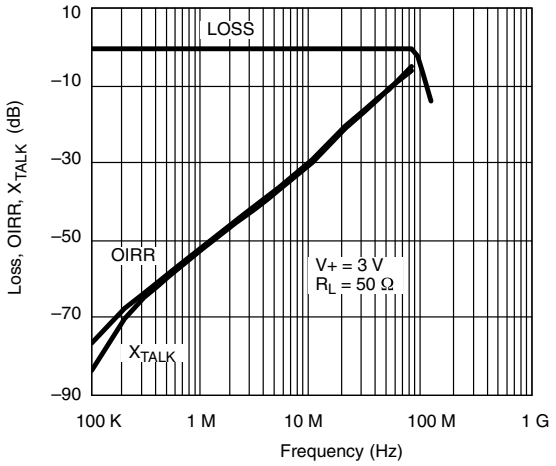


Switching Time vs. Temperature and Supply Voltage

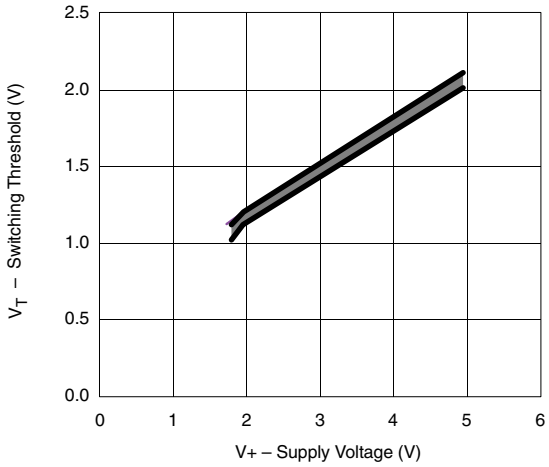
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



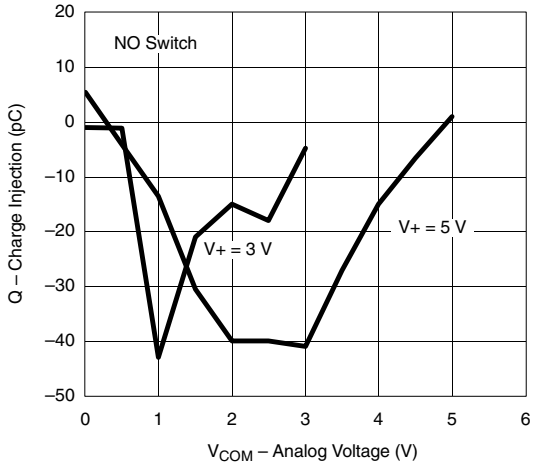
Switching Time vs. Temperature and Supply Voltage



Insertion Loss, Off-Isolation Crosstalk vs. Frequency

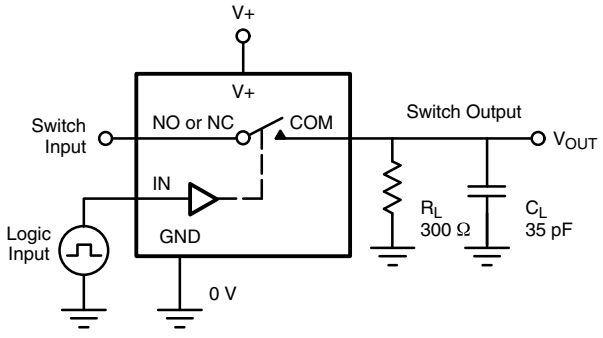


Switching Threshold vs. Supply Voltage



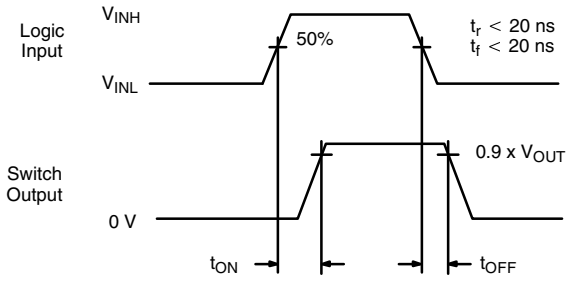
Charge Injection vs. Analog Voltage

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

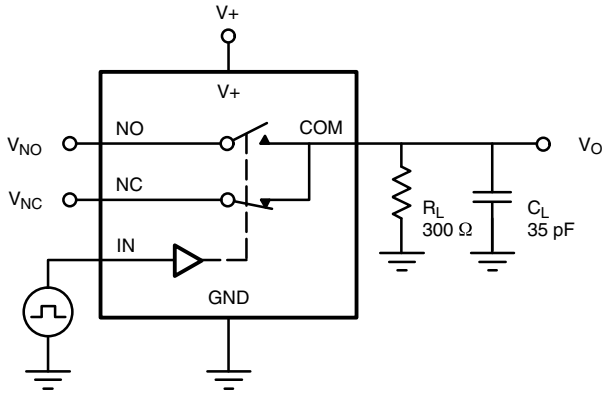
$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Fig. 1 - Switching Time

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

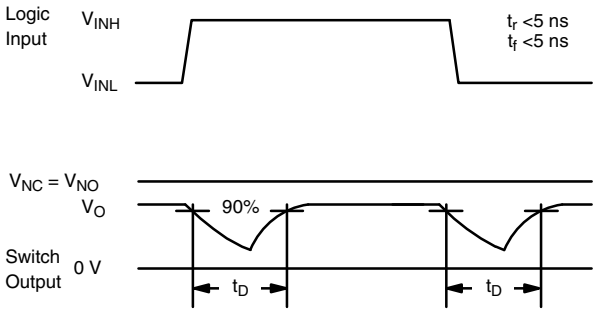
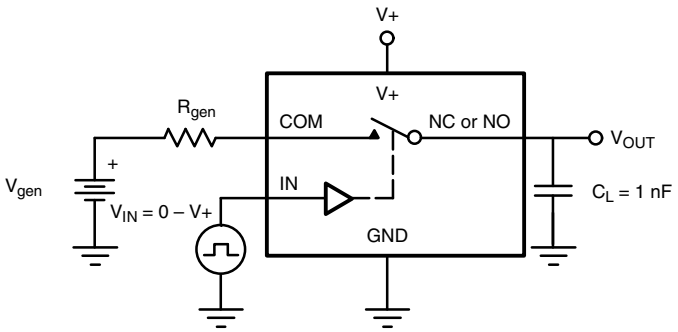
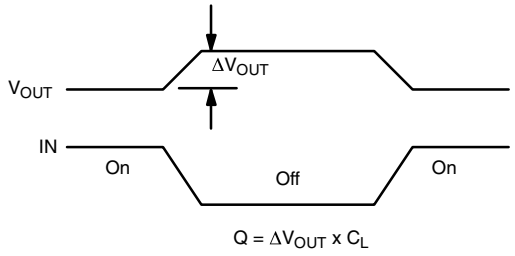


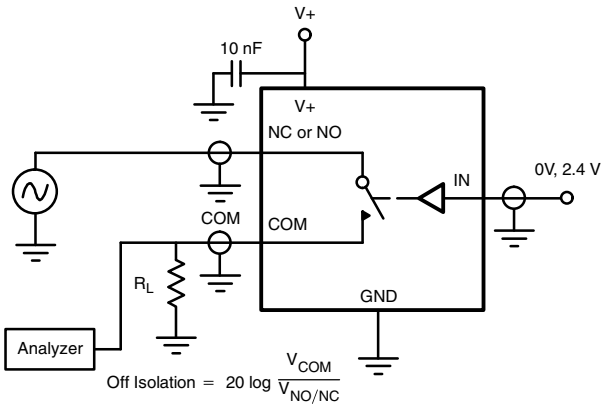
Fig. 2 - Break-Before-Make Interval





IN depends on switch configuration: input polarity determined by sense of switch.

Fig. 3 - Charge Injection



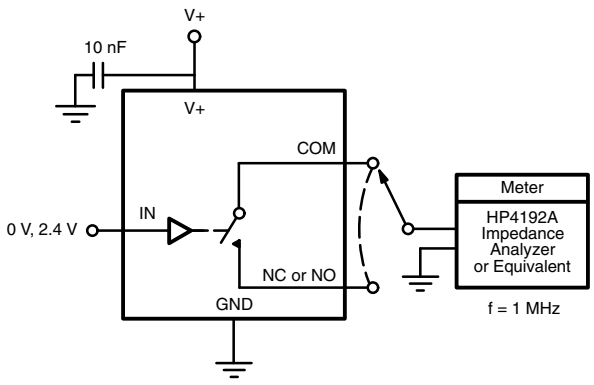
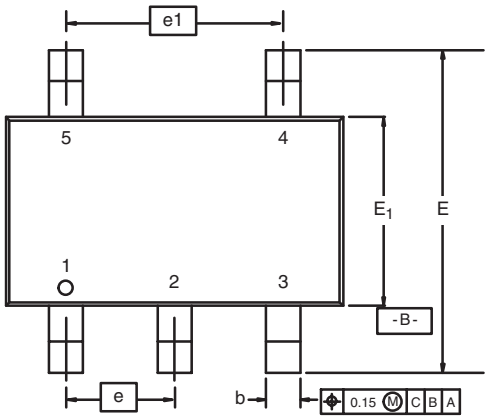


Fig. 4 - Off-Isolation

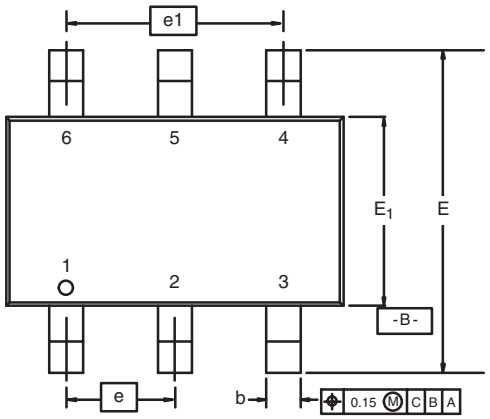
Fig. 5 - Channel off/on Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71676.

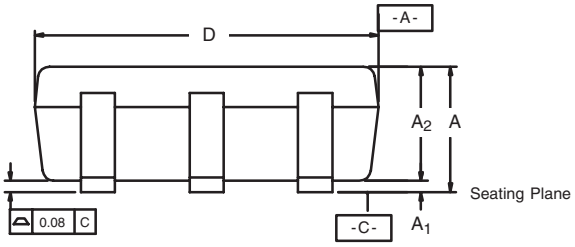
TSOP: 5/6–LEAD
JEDEC Part Number: MO-193C

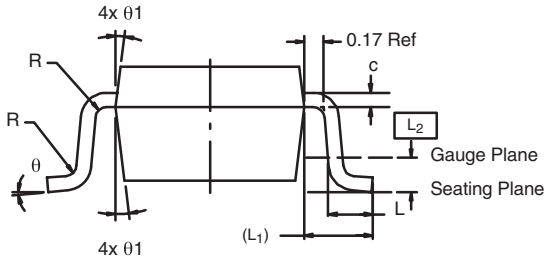


5-LEAD TSOP



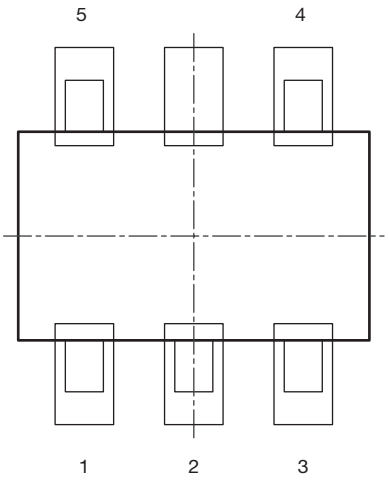
6-LEAD TSOP



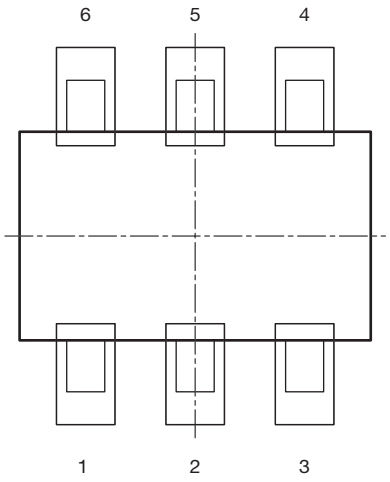


Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A_1	0.01	-	0.10	0.0004	-	0.004
A_2	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E_1	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e_1	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L_1	0.60 Ref			0.024 Ref		
L_2	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ_1	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540						

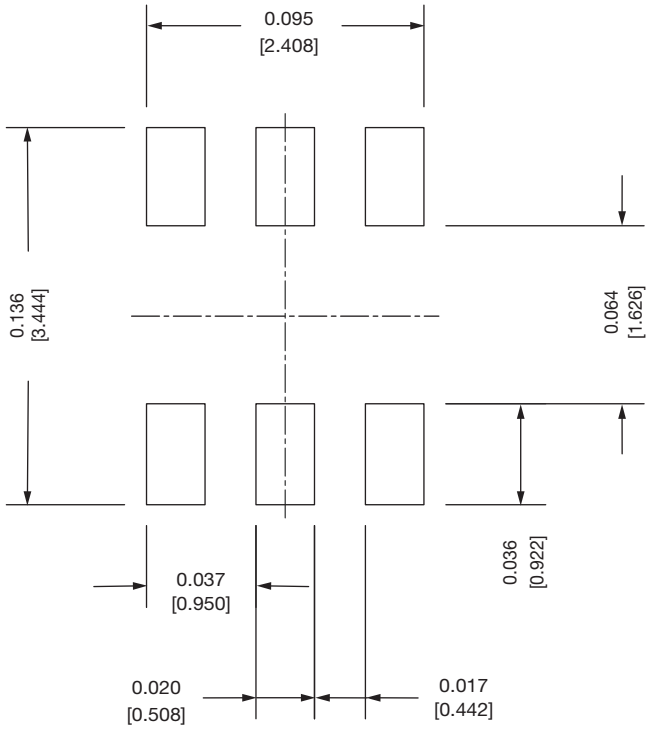
Recommended Land Pattern For TSOP-5L / TSOP-6L



TSOP 5L



TSOP 6L



Note

- All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022 DWG: 3010

Disclaimer

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