

N-Channel 80 V (D-S) 175 °C MOSFET

DESCRIPTION

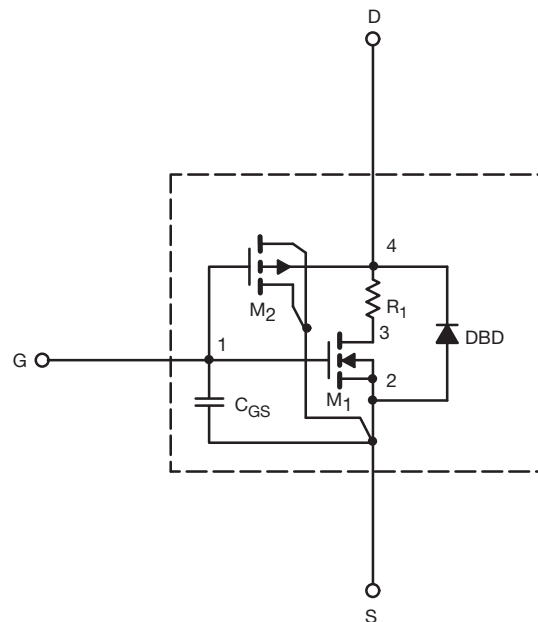
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



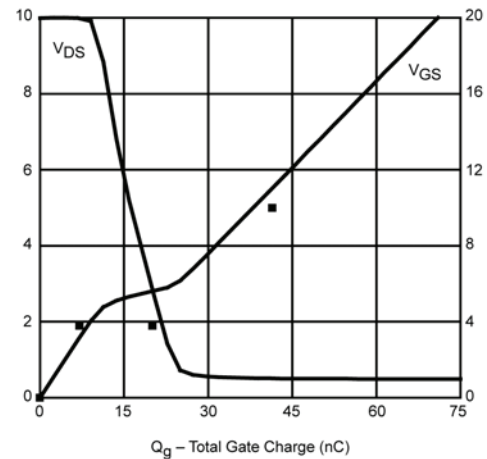
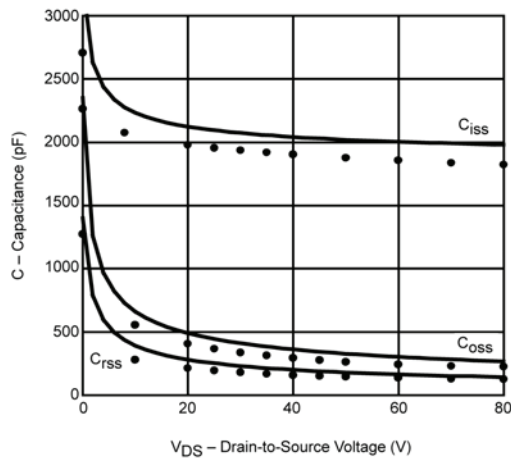
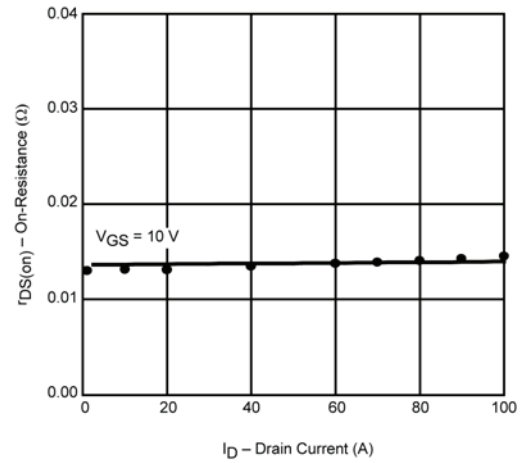
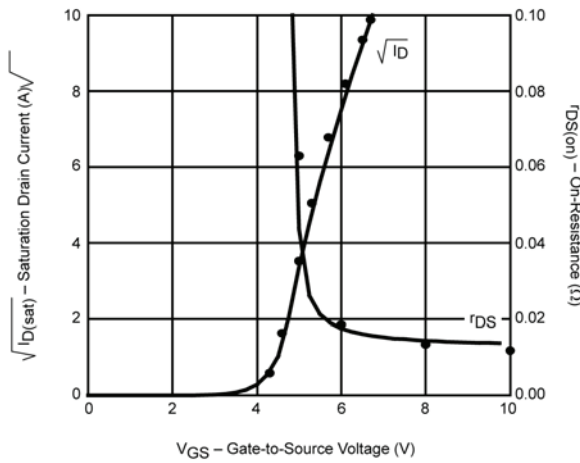
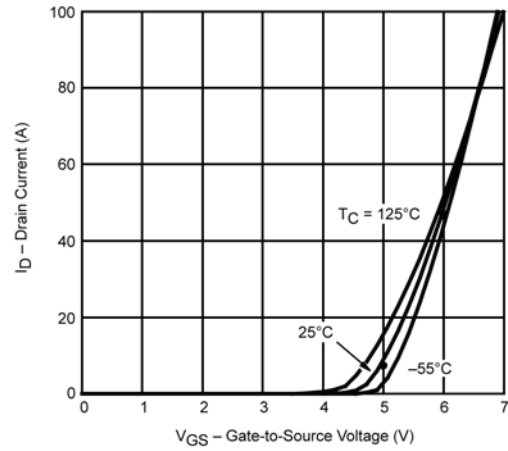
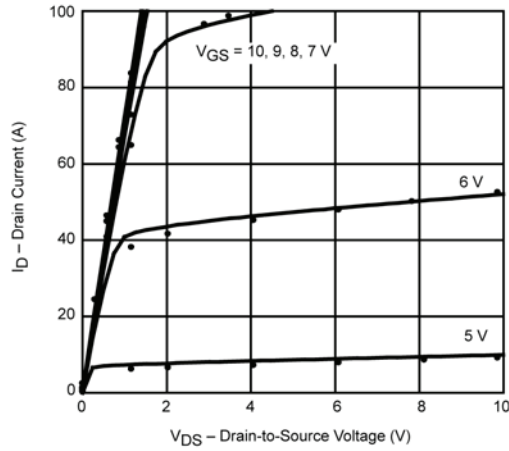
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	3.4	-	V
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	304	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 40 A	0.013	0.013	Ω
		V _{GS} = 10 V, I _D = 40 A, T _J = 125 °C	0.022	-	
		V _{GS} = 10 V, I _D = 40 A, T _J = 175 °C	0.026	-	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 40 A	49	45	S
Diode Forward Voltage	V _{SD}	I _S = 40 A, V _{GS} = 0 V	0.91	1	V
Dynamic^b					
Input Capacitance	C _{iss}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	2091	1960	pF
Output Capacitance	C _{oss}		438	370	
Reverse Transfer Capacitance	C _{rss}		248	200	
Total Gate Charge	Q _g	V _{DS} = 40 V, V _{GS} = 10 V, I _D = 40 A	39	42	nC
Gate-Source Charge	Q _{gs}		7	7	
Gate-Drain Charge	Q _{gd}		13	13	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 40 V, R _L = 1 Ω I _D = 40 A, V _{GEN} = 10 V, R _g = 2.5 Ω	19	12	ns
Rise Time	t _r		29	52	
Turn-Off Delay Time	t _{d(off)}		31	25	
Fall Time	t _f		40	10	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = 40 A, di/dt = 100 A/μs	38	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

- Dots and squares represent measured data.



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