P-Channel 60-V (D-S) MOSFET

CHARACTERISTICS

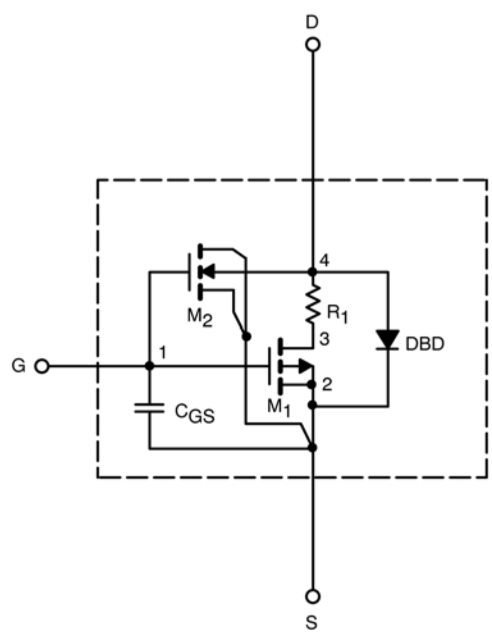
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

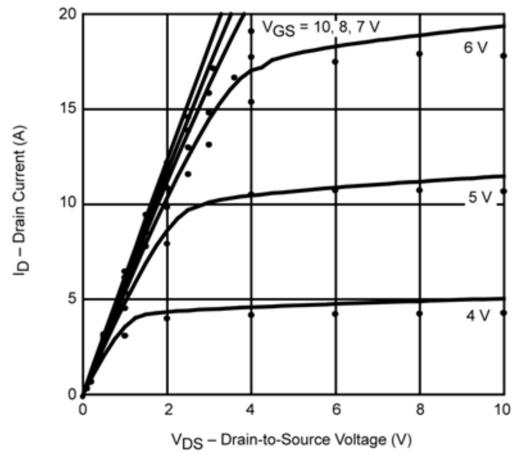


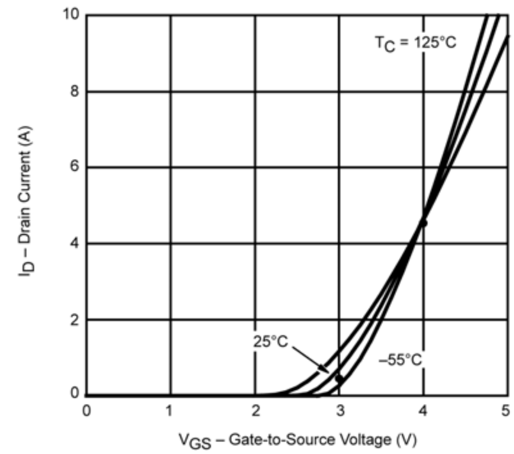
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

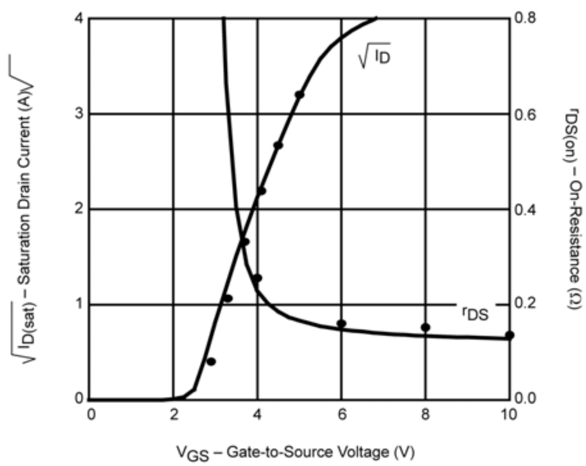
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)				
Parameter	**Symbol**	**Test Condition**	**Typical**	**Unit**
Static				
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = –250 μA	2.1	V
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = – 5 V, V_{GS} = –10 V	47	A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = –10 V, I_D = –5 A	0.15	Ω
		V_{GS} = –4.5 V, I_D = –2 A	0.21	
		V_{GS} = –10 V, I_D = –5 A, T_j = 125°C	0.28	
		V_{GS} = –10 V, I_D = –5 A, T_j = 175°C	0.35	
Forward Transconductance[a]	g_{fs}	V_{DS} = –15 V, I_D = –5 A	5.7	S
Diode Forward Voltage[a]	V_{SD}	I_S = –10 A, V_{GS} = 0 V	0.87	V
Dynamic				
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = –25 V, f = 1 MHz	639	pf
Output Capacitance	C_{oss}		105	
Reverse Transfer Capacitance	C_{rss}		45	
Total Gate Charge[b]	Q_g	V_{DS} = –30 V, V_{GS} = –10 V, I_D = –10 A	10.5	nC
Gate-Source Charge[b]	Q_{gs}		4	
Gate-Drain Charge[b]	Q_{gd}		2	
Turn-On Delay Time[b]	$t_{d(on)}$	V_{DD} = –30 V, R_L = 3 Ω I_D ≅ –10 A, V_{GEN} = –10 V, R_G = 2.5 Ω	4.3	ns
Rise Time[b]	t_r		15.2	
Turn-Off Delay Time[b]	$t_{d(off)}$		15	
Fall Time[b]	t_f		5.6	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = –10 A, di/dt = 100 A/μs	47	

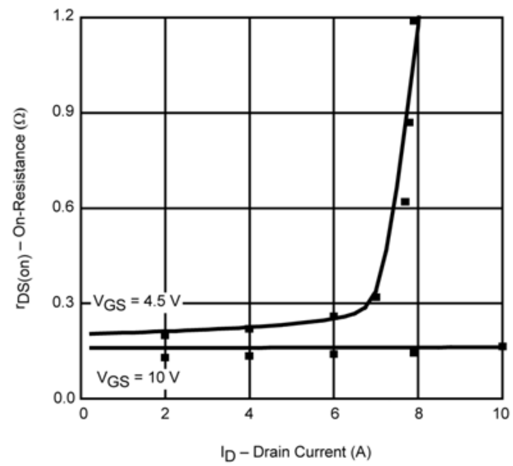
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%
b. Independent of operating temperature.

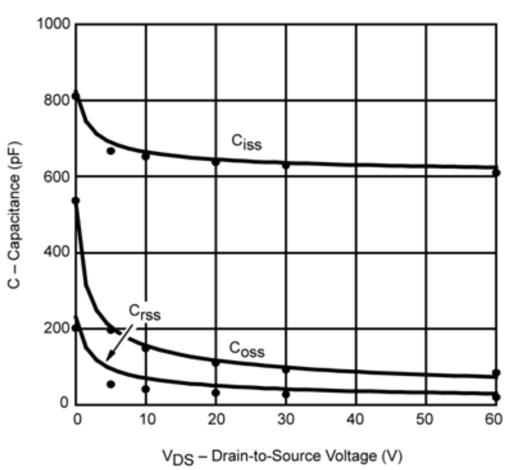
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

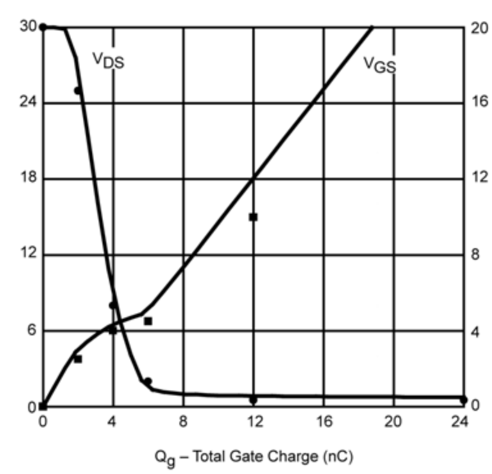












Note: Dots and squares represent measured data.

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