



## N-Channel 60-V (D-S), 175°C MOSFET, Logic Level

### CHARACTERISTICS

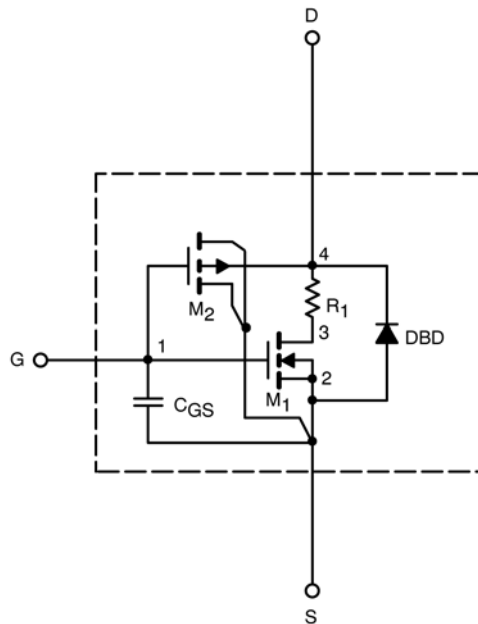
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0 to 5V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

# SPICE Device Model SUD25N06-45L

Vishay Siliconix



SPECIFICATIONS (T <sub>J</sub> = 25°C UNLESS OTHERWISE NOTED)				
Parameter	Symbol	Test Conditions	Typical	Unit
<b>Static</b>				
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.99	V
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	170	A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 12 A	0.027	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 12 A, T <sub>J</sub> = 125°C	0.058	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 12 A, T <sub>J</sub> = 175°C	0.075	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 12 A	0.041	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 12 A	18	S
Diode Forward Voltage <sup>b</sup>	V <sub>SD</sub>	I <sub>S</sub> = 25 A, V <sub>GS</sub> = 0 V	0.89	V
<b>Dynamic</b>				
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz	1245	pf
Output Capacitance	C <sub>oss</sub>		226	
Reverse Transfer Capacitance	C <sub>rss</sub>		70	
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 25 A	24	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>		7.5	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>		4.5	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 1.2 Ω I <sub>D</sub> ≅ 25 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 7.5 Ω	9.3	ns
Rise Time <sup>c</sup>	t <sub>r</sub>		15	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>		22	
Fall Time <sup>c</sup>	t <sub>f</sub>		31	
Source-Drain Reverse Recovery Time <sup>b</sup>	t <sub>rr</sub>	I <sub>F</sub> = 25 A, di/dt = 100 A/μs	56	

**Notes**

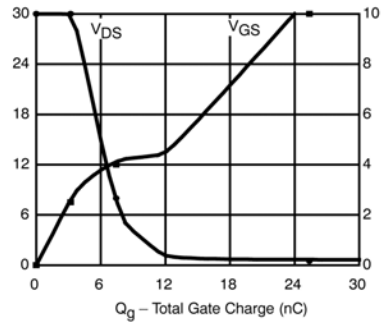
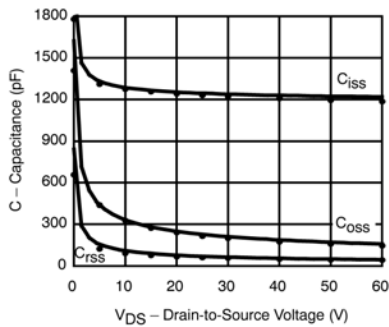
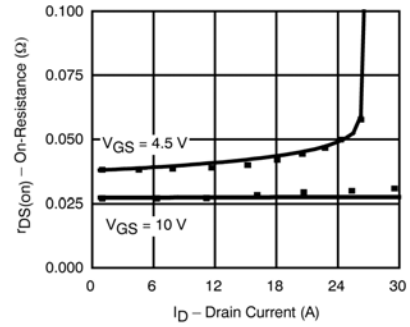
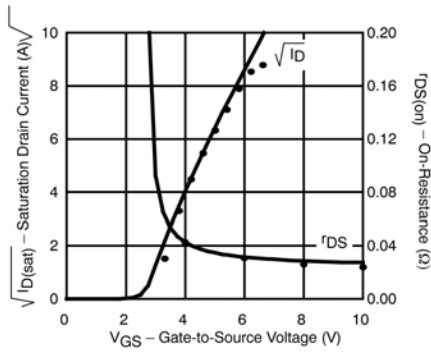
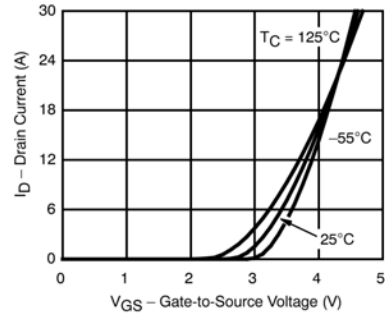
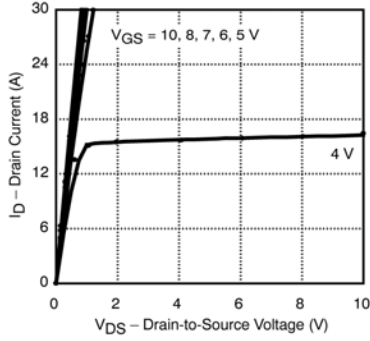
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. For design aid only; not subject to production testing
- c. Independent of operating temperature



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COMPARISON OF MODEL WITH MEASURED DATA ( $T_J=25^\circ\text{C}$  UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



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