



P-Channel 8-V (D-S), 175°C MOSFET

CHARACTERISTICS

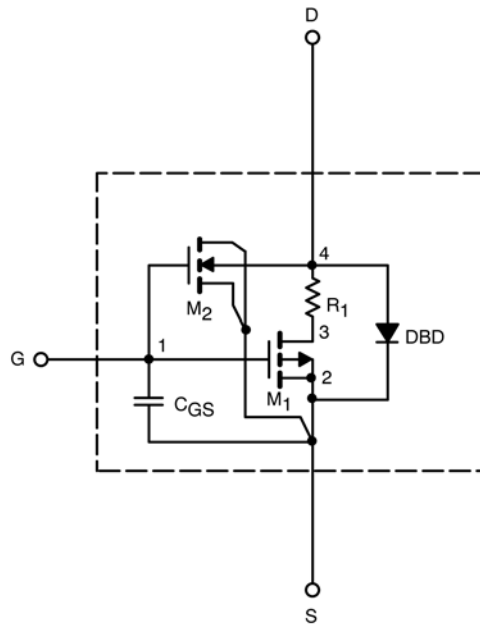
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	0.83		V
On-State Drain Current ^a	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -4.5 V	42		A
		V _{DS} = -5 V, V _{GS} = -2.5 V	11		
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -10 A	0.070	0.043	Ω
		V _{GS} = -4.5 V, I _D = -10 A, T _J = 125°C	0.092		
		V _{GS} = -4.5 V, I _D = -10 A, T _J = 175°C	0.105		
		V _{GS} = -2.5 V, I _D = -5 A	0.106		
		V _{GS} = -1.8 V, I _D = -2 A	0.159		
Forward Voltage ^a	V _{SD}	I _F = -15 A, V _{GS} = 0 V	-0.88		V
Dynamic^b					
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = -4 V, f = 1 MHz	1304	1300	pF
Output Capacitance	C _{oss}		445	430	
Reverse Transfer Capacitance	C _{rss}		271	245	
Total Gate Charge ^c	Q _g	V _{DS} = -4 V, V _{GS} = -4.5 V, I _D = -10 A	10.3	10.5	nC
Gate-Source Charge ^c	Q _{gs}		1.6	1.6	
Gate-Drain Charge ^c	Q _{gd}		2	2	
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = -4 V, R _L = 0.22 Ω I _D ≅ -15 A, V _{GEN} = -4.5 V, R _G = 2.5 Ω	12	10	ns
Rise Time ^c	t _r		19	16	
Turn-Off Delay Time ^c	t _{d(off)}		27	30	
Fall Time ^c	t _f		21	25	
Reverse Recovery Time	t _{rr}	I _F = -15 A, di/dt = 100 A/μs	32	45	

Notes

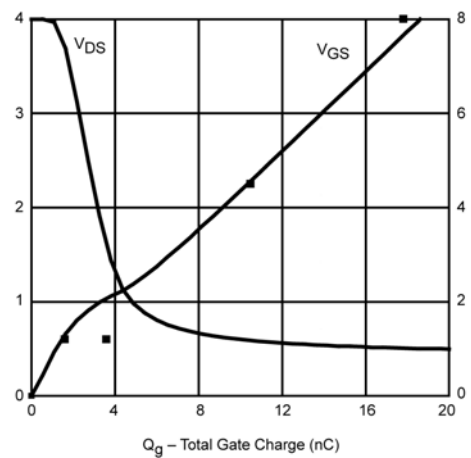
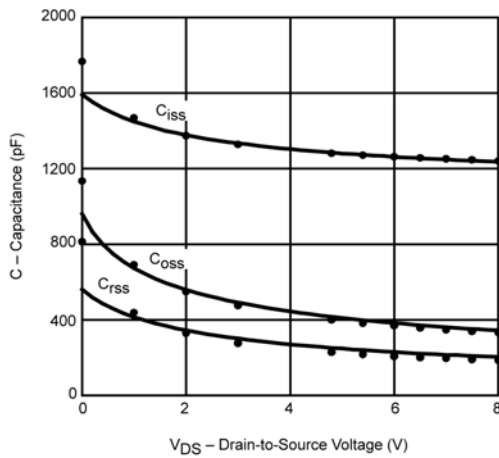
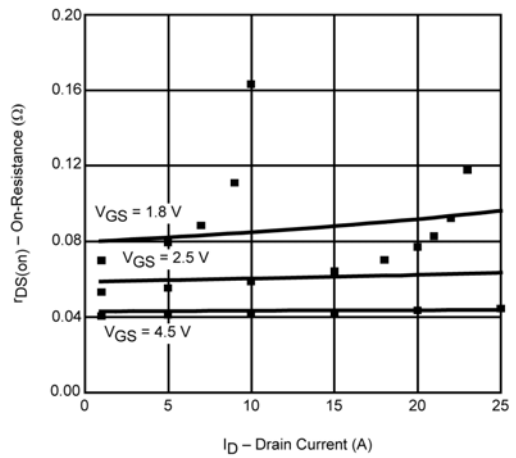
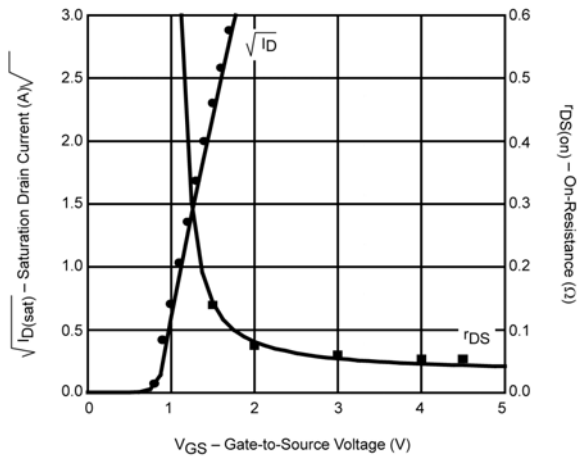
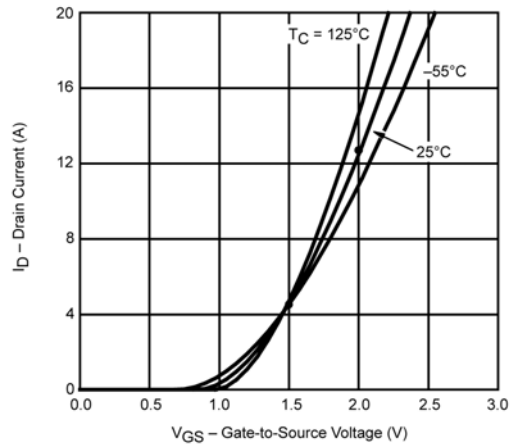
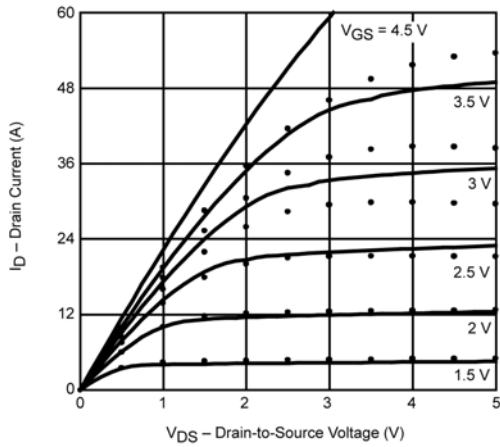
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.



SPICE Device Model SUD15P01-52

Vishay Siliconix

COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



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