



N- and P-Channel MOSFET

CHARACTERISTICS

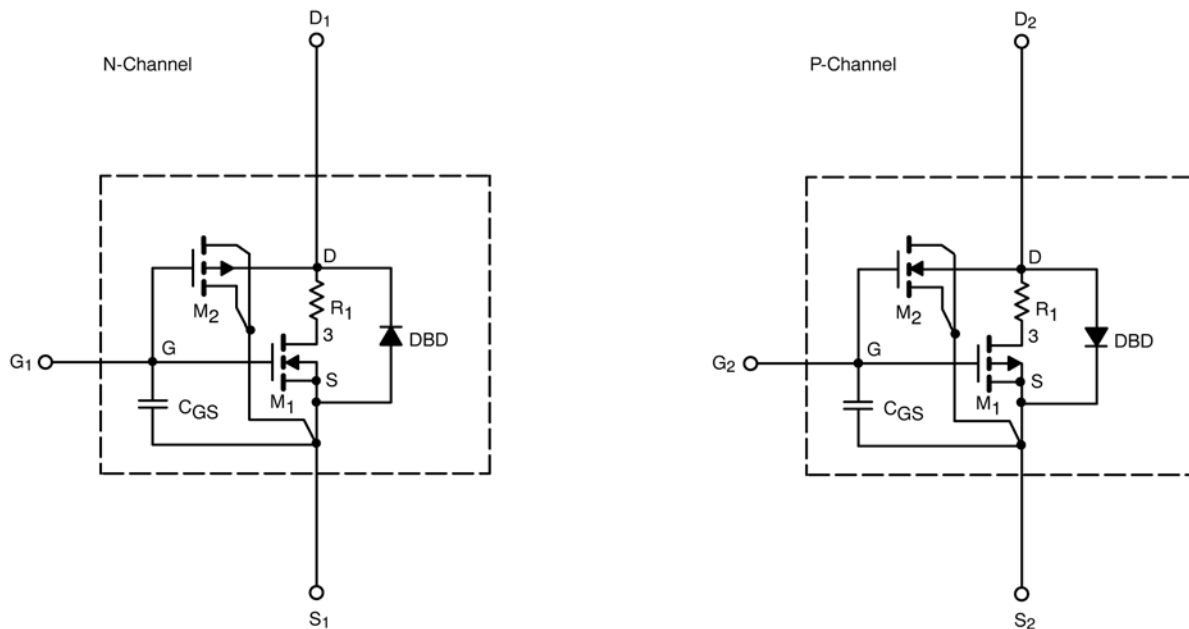
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

SPICE Device Model Si4505DY



Vishay Siliconix

SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Condition		Simulated Data	Measured Data	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1.4			
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	0.87			
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	N-Ch	273		A	
		V _{DS} = -5 V, V _{GS} = -4.5 V	P-Ch	64			
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 7.8 A	N-Ch	0.014	0.015	Ω	
		V _{GS} = -4.5 V, I _D = -5 A	P-Ch	0.032	0.030		
		V _{GS} = 4.5 V, I _D = 6.4 A	N-Ch	0.020	0.022		
		V _{GS} = -2.5 V, I _D = -4 A	P-Ch	0.052	0.048		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 7.8 A	N-Ch	21	18	S	
		V _{DS} = -15 V, I _D = -5 A	P-Ch	16	12		
Diode Forward Voltage ^a	V _{SD}	I _S = 1.8 A, V _{GS} = 0 V	N-Ch	0.72	0.73	V	
		I _S = -1.8 A, V _{GS} = 0 V	P-Ch	0.81	-0.75		
Dynamic^b							
Total Gate Charge	Q _g	N-Channel V _{DS} = 15 V, V _{GS} = 5 V, I _D = 7.8 A P-Channel V _{DS} = -4 V, V _{GS} = -5 V, I _D = -5 A	N-Ch	11.8	11.5	nC	
Gate-Source Charge	Q _{gs}		P-Ch	13.3	13.5		
			N-Ch	3	3		
Gate-Source Charge	Q _{gs}		P-Ch	2.2	2.2		
			N-Ch	4	4		
			P-Ch	3	3		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω P-Channel V _{DD} = -4 V, R _L = 4 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _G = Ω	N-Ch	12	15	ns	
			P-Ch	26	21		
Rise Time	t _r		N-Ch	10	8		
			P-Ch	31	45		
Turn-Off Delay Time	t _{d(off)}		N-Ch	17	35		
			P-Ch	23	60		
Fall Time	t _f		N-Ch	17	10		
			P-Ch	39	55		
Source-Drain Reverse Recovery Time	t _{rr}		I _S = 1.8A, di/dt = 100 A/μs	N-Ch	22		30
				P-Ch	34		50

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

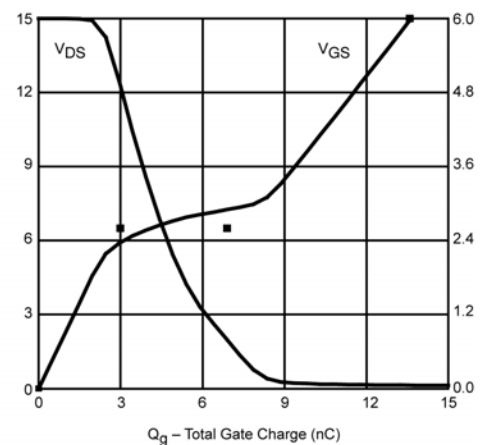
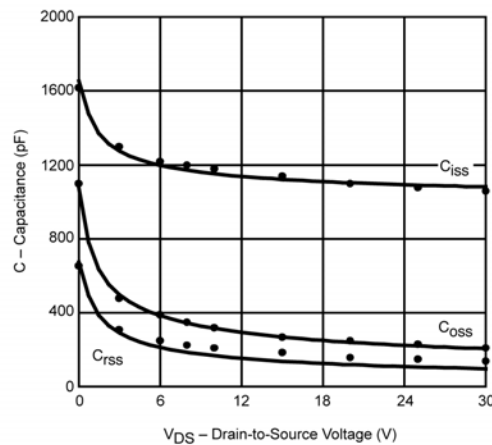
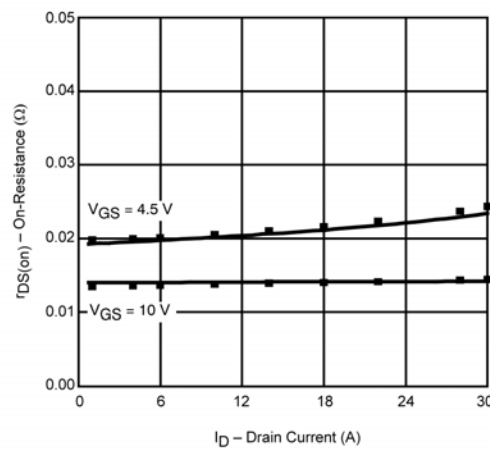
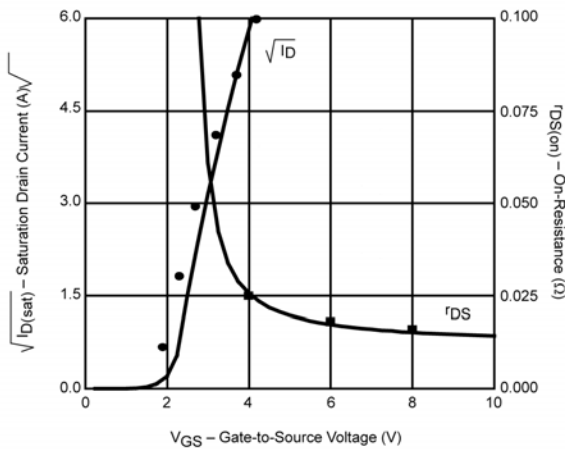
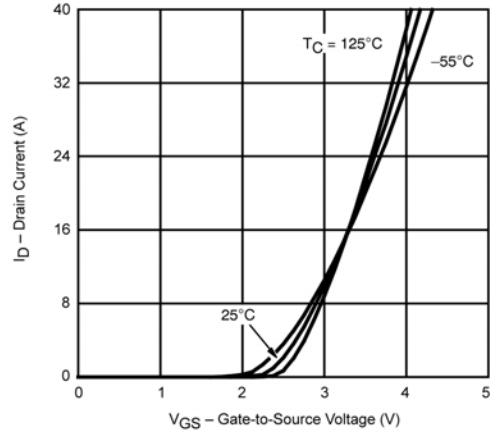
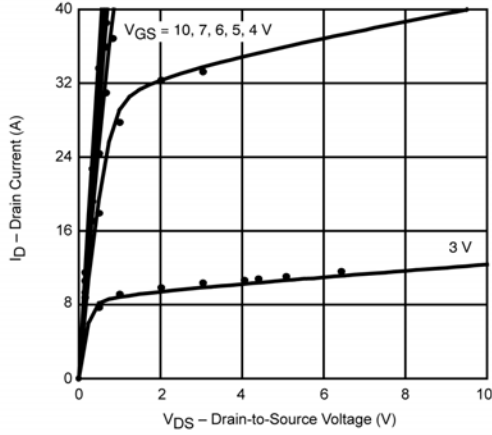


SPICE Device Model Si4505DY

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COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

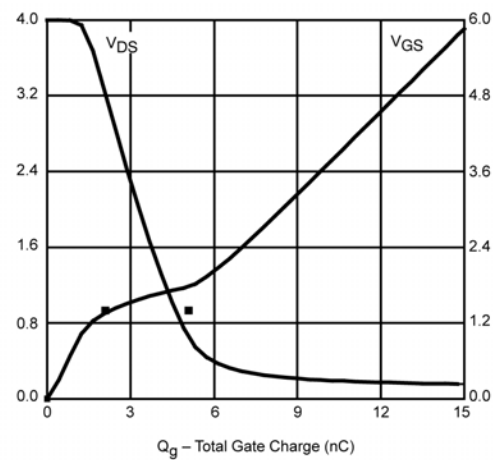
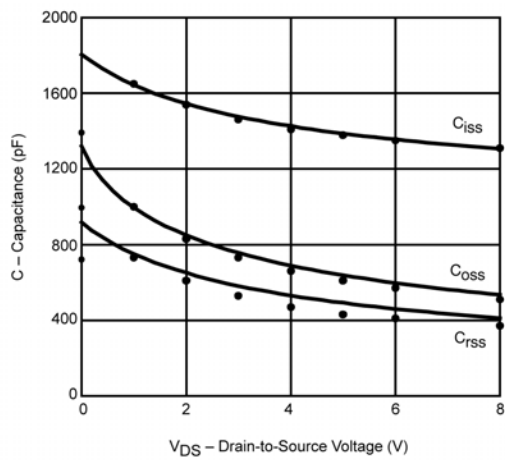
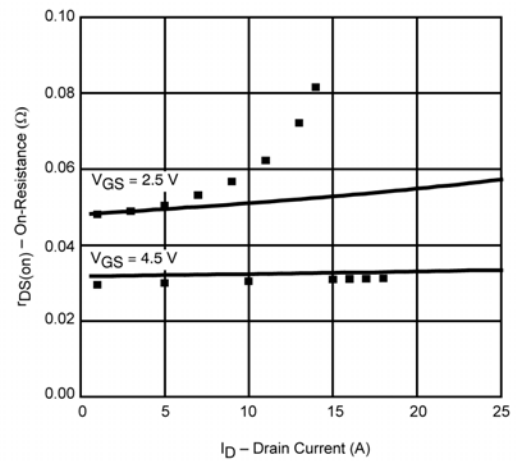
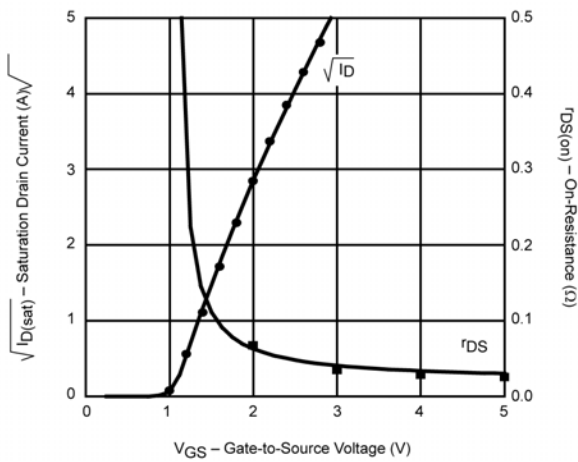
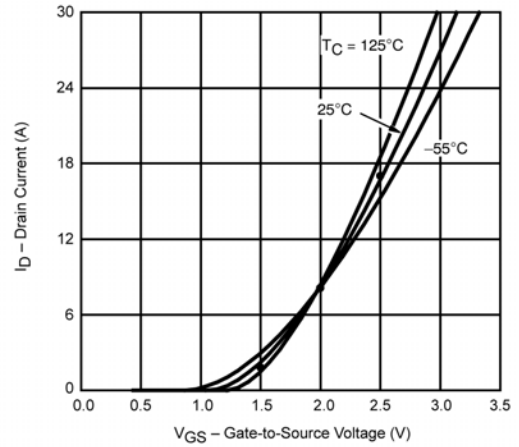
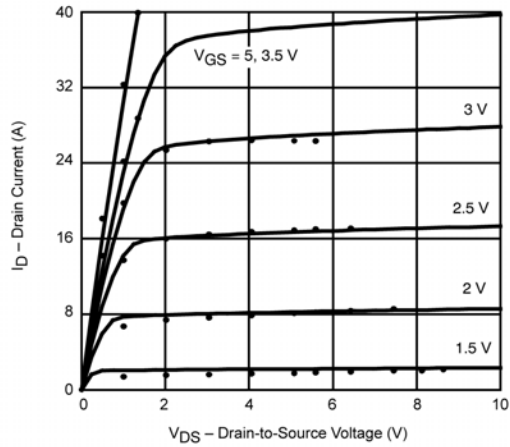
N-Channel MOSFET



Note: Dots and squares represent measured data.



P-Channel MOSFET



Note: Dots and squares represent measured data.



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