

N-Channel 100 V (D-S) 175 °C MOSFET

DESCRIPTION

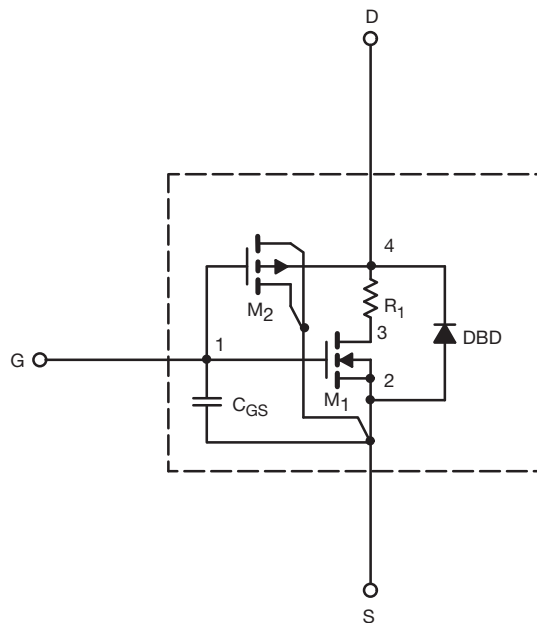
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



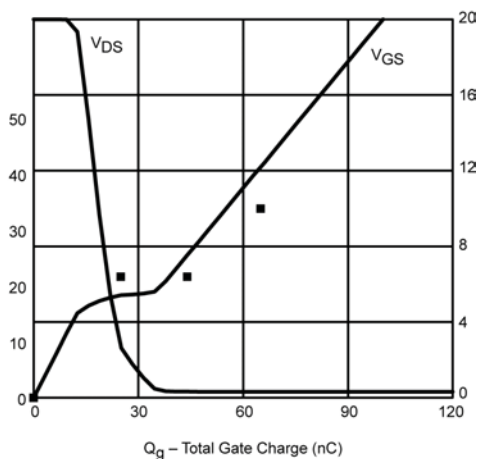
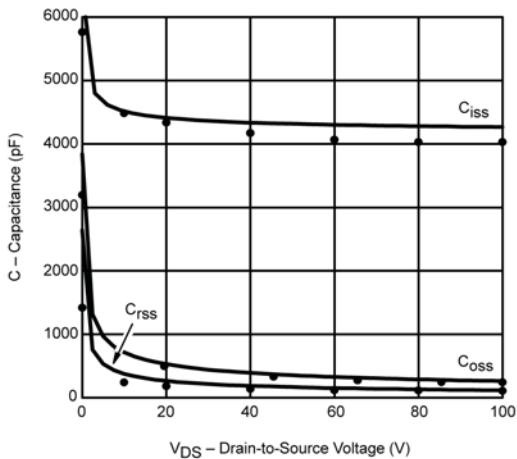
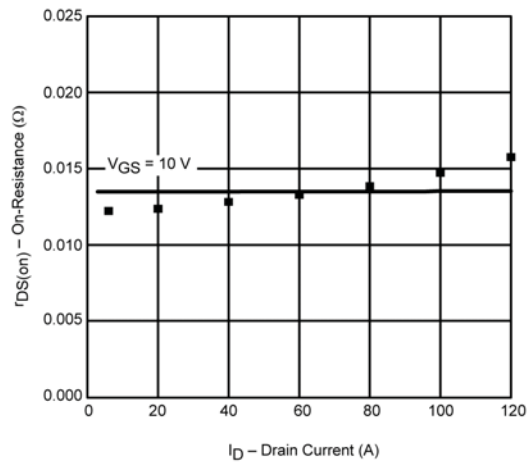
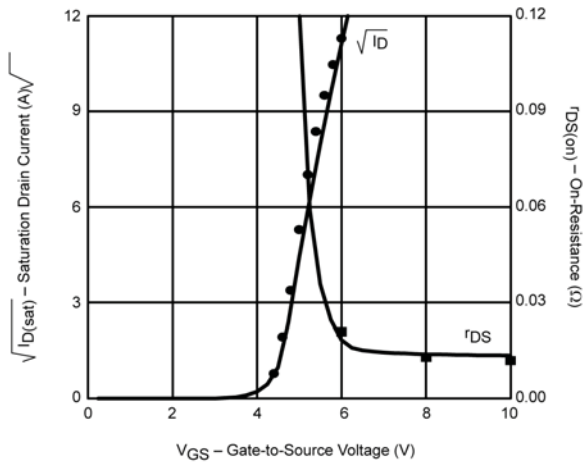
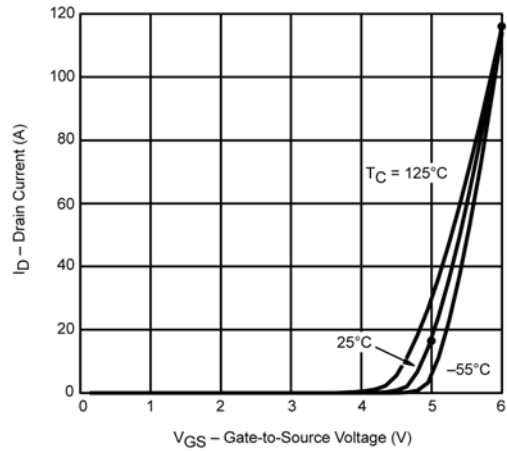
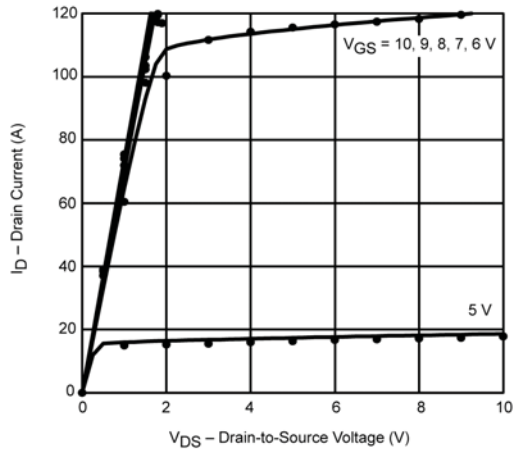
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.2	-	V
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 10\ \text{V}$	366	-	A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 30\ \text{A}$	0.013	0.013	Ω
		$V_{GS} = 6\ \text{V}, I_D = 20\ \text{A}$	0.015	0.015	
		$V_{GS} = 10\ \text{V}, I_D = 30\ \text{A}, T_J = 125\text{ }^\circ\text{C}$	0.024	-	
		$V_{GS} = 10\ \text{V}, I_D = 30\ \text{A}, T_J = 175\text{ }^\circ\text{C}$	0.030	-	
Diode Forward Voltage	V_{SD}	$I_F = 30\ \text{A}, V_{GS} = 0\ \text{V}$	0.9	1	V
Dynamic^b					
Input Capacitance	C_{iss}	$V_{DS} = 25\ \text{V}, V_{GS} = 0\ \text{V}, f = 1\ \text{MHz}$	4377	4300	pF
Output Capacitance	C_{oss}		482	450	
Reverse Transfer Capacitance	C_{rss}		239	175	
Total Gate Charge	Q_g	$V_{DS} = 50\ \text{V}, V_{GS} = 10\ \text{V}, I_D = 60\ \text{A}$	57	65	nC
Gate-Source Charge	Q_{gs}		25	25	
Gate-Drain Charge	Q_{gd}		19	19	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\ \text{V}, R_L = 1.5\ \Omega$ $I_D = 60\ \text{A}, V_{GEN} = 10\ \text{V}, R_g = 2.5\ \Omega$	25	15	ns
Rise Time	t_r		12	12	
Turn-Off Delay Time	$t_{d(off)}$		17	30	
Fall Time	t_f		10	10	
Source-Drain Reverse Recovery Time	t_{rr}		$I_F = 50\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$	110	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\ \%$.
b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

- Dots and squares represent measured data.



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