

P-Channel 1.8 V (G-S) MOSFET

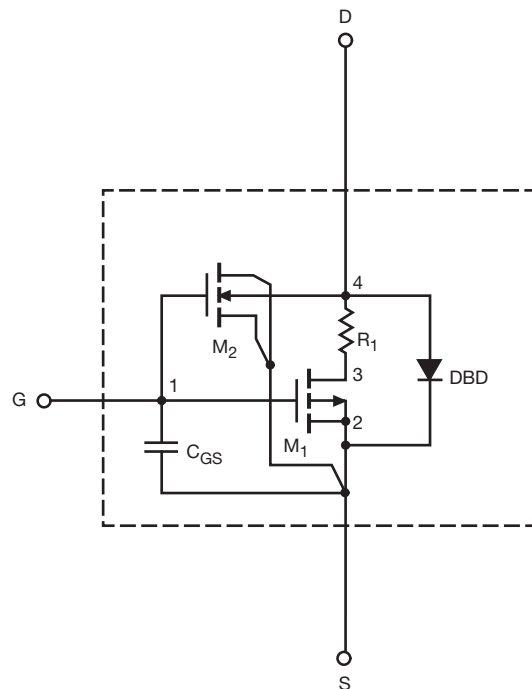
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



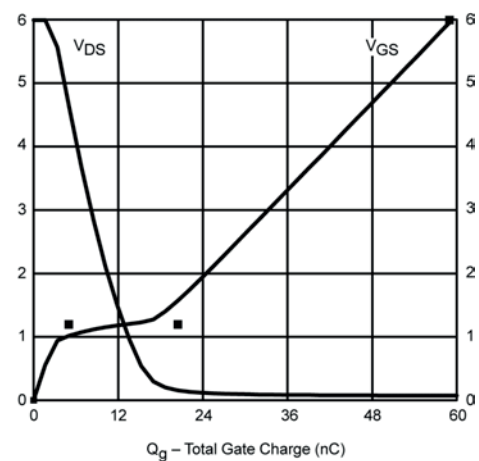
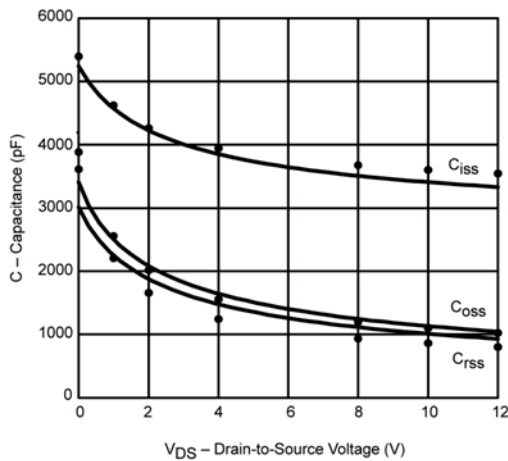
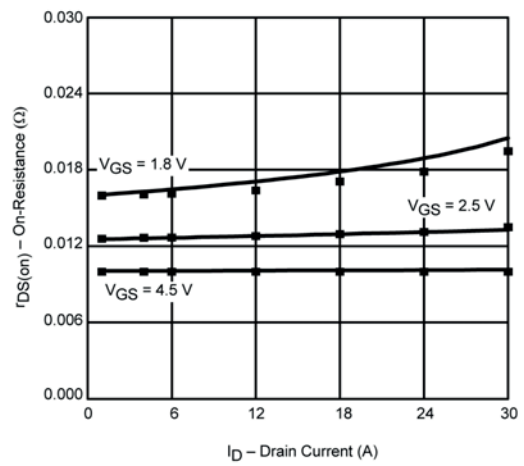
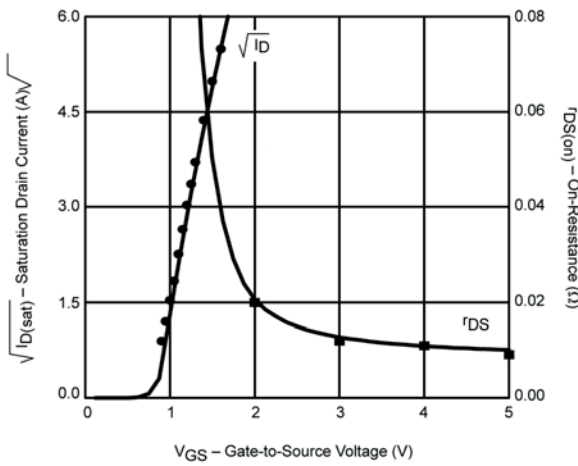
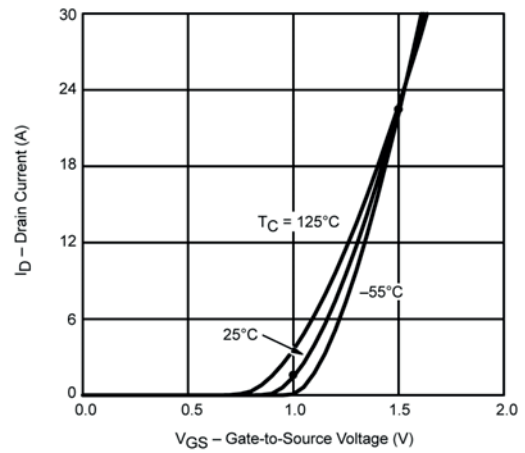
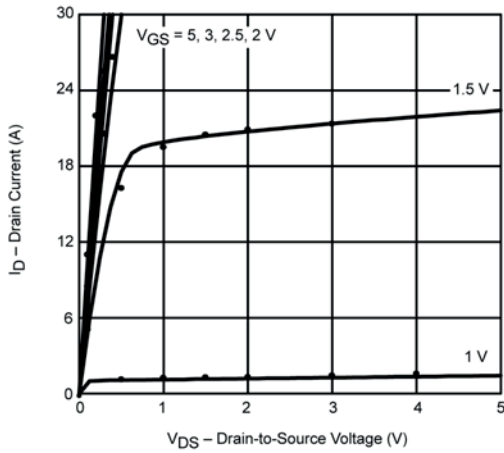
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	0.63	-	V
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\text{ V}, V_{GS} = -4.5\text{ V}$	312	-	A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -8\text{ A}$	0.010	0.010	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -7\text{ A}$	0.0127	0.0125	
		$V_{GS} = -1.8\text{ V}, I_D = -5.8\text{ A}$	0.0165	0.016	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -5\text{ V}, I_D = -8\text{ A}$	40	44	S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.5\text{ A}, V_{GS} = 0\text{ V}$	-0.80	-0.56	V
Dynamic^b					
Total Gate Charge	Q_g	$V_{DS} = -6\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -8\text{ A}$	46	46	nC
Gate-Source Charge	Q_{gs}		5	5	
Gate-Drain Charge	Q_{gd}		15.5	15.5	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\text{ V}, R_L = 6\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 6\text{ }\Omega$	44	45	ns
Rise Time	t_r		42	85	
Turn-Off Delay Time	$t_{d(off)}$		169	220	
Fall Time	t_f		142	155	

Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

- Dots and squares represent measured data.



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