P-Channel 30-V (D-S) MOSFET

CHARACTERISTICS

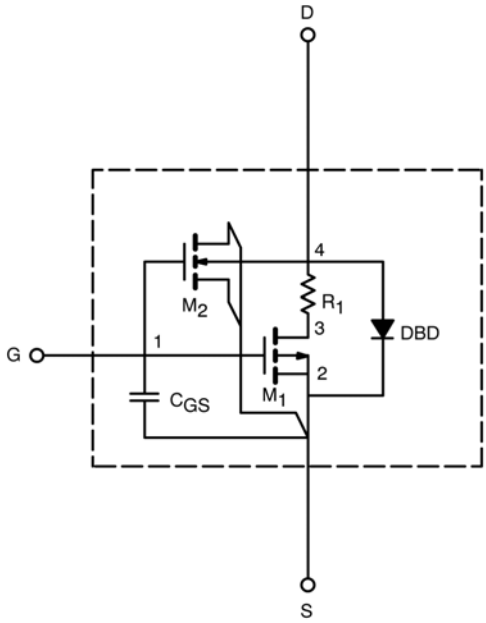
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the –55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit mode is extracted and optimized over the –55 to 125°C temperature ranges under the pulsed 0-to-10V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

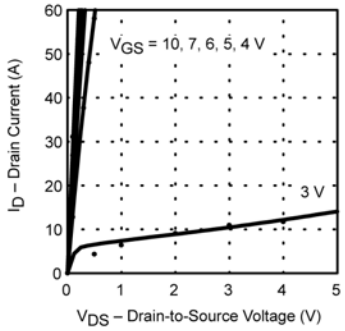


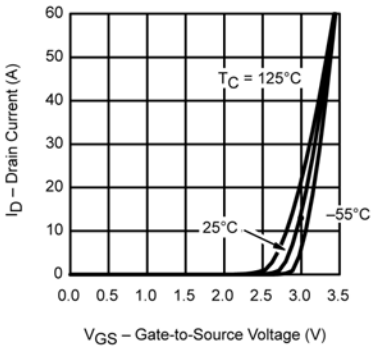
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

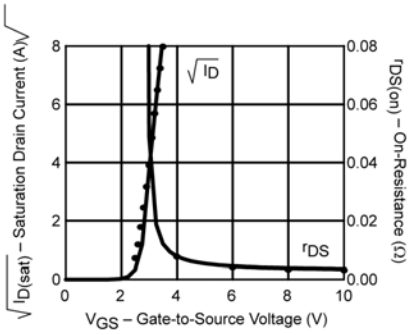
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	**Symbol**	**Test Conditions**	**Simulated Data**	**Measured Data**	**Unit**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\mu A$	2		V
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} = -5V$, $V_{GS} = -10V$	1299		A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	$V_{GS} = -10V$, $I_D = -24A$	0.0035	0.0036	Ω
		$V_{GS} = -4.5V$, $I_D = -17A$	0.006	0.006	
Forward Transconductance[a]	g_{fs}	$V_{DS} = -15V$, $I_D = -24A$	122	80	S
Diode Forward Voltage[a]	V_{SD}	$I_S = -2.9A$, $V_{GS} = 0V$	- 0.83	- 0.71	V
Dynamic[b]					
Total Gate Charge	Q_g	$V_{DS} = -15V$, $V_{GS} = -10V$, $I_D = -24A$	139	146	nC
Gate-Source Charge	Q_{gs}		20	20	
Gate-Drain Charge	Q_{gd}		41	41	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15V$, $R_L = 15\Omega$ $I_D \cong -1A$, $V_{GEN} = -10V$, $R_G = 6\Omega$	32	30	ns
Rise Time	t_r		36	25	
Turn-Off Delay Time	$t_{d(off)}$		124	235	
Fall Time	t_f		111	130	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.9A$, di/dt = 100A/μs	74	100	

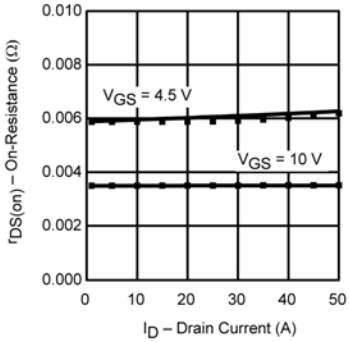
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

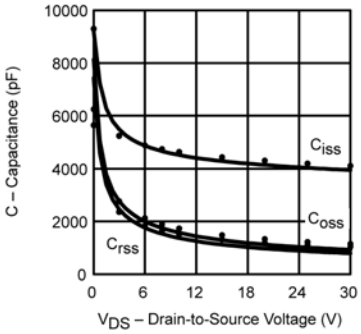
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

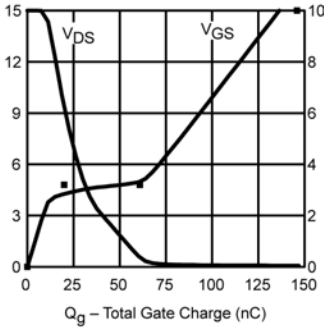












Note: Dots and squares represent measured data.

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