N-Channel 240 V (D-S) MOSFET

FEATURES

• Low On-Resistance: 4 Ω
• Secondary Breakdown Free: 260 V
• Low Power/Voltage Driven
• Low Input and Output Leakage
• Excellent Thermal Stability
• Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

• High-Voltage Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Transistors, etc.
• Telephone Mute Switches, Ringer Circuits
• Power Supply, Converters
• Motor Control

BENEFITS

• Low Offset Voltage
• Full-Voltage Operation
• Easily Driven Without Buffer
• Low Error Voltage
• No High-Temperature “Run-Away”

ABSOLUTE MAXIMUM RATINGS (TA = 25 °C, unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>TN2404K</th>
<th>TN2404KL/BS107KL</th>
<th>Symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-Source Voltage</td>
<td>VDS</td>
<td>240</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Gate-Source Voltage</td>
<td>VGS</td>
<td>± 20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Continuous Drain Current (TJ = 150 °C)</td>
<td>I_D</td>
<td>0.2</td>
<td>0.3</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.16</td>
<td>0.25</td>
<td>A</td>
</tr>
<tr>
<td>Pulsed Drain Current (t = 300 µs)</td>
<td>I_DM</td>
<td>0.8</td>
<td>1.4</td>
<td></td>
</tr>
<tr>
<td>Maximum Power Dissipation</td>
<td>P_D</td>
<td>0.36</td>
<td>0.8</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.23</td>
<td>0.51</td>
<td>W</td>
</tr>
<tr>
<td>Thermal Resistance Junction-to-Ambient</td>
<td>RthJA</td>
<td>350b</td>
<td>156</td>
<td>°C/W</td>
</tr>
<tr>
<td>Operating Junction and Storage Temperature Range</td>
<td>T_J, Tslg</td>
<td>- 55 to 150</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
a. Pulse width limited by maximum junction temperature.
b. Surface mounted on an FR4 board.
## SPECIFICATIONS (T_A = 25 °C, unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static</strong></td>
<td></td>
<td></td>
<td>Min.</td>
</tr>
<tr>
<td>Drain-Source Breakdown Voltage</td>
<td>V_DS</td>
<td>V_GS = 0 V, I_D = 100 µA</td>
<td>240</td>
</tr>
<tr>
<td>Gate-Source Threshold Voltage</td>
<td>V_GS(th)</td>
<td>V_DS = V_GS, I_D = 250 µA</td>
<td>0.8</td>
</tr>
<tr>
<td>Gate-Source Leakage</td>
<td>I_GSS</td>
<td>V_DS = 0 V, V_GS = ± 20 V</td>
<td>± 100</td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current</td>
<td>I_DSS</td>
<td>V_DS = 192 V, V_GS = 0 V</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DS = 192 V, V_GS = 0 V, T_J = 55 °C</td>
<td>10</td>
</tr>
<tr>
<td>On-State Drain Current</td>
<td>I_D(on)</td>
<td>V_DS = 10 V, V_GS = 10 V</td>
<td>0.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DS = 10 V, V_GS = 4.5 V</td>
<td>0.5</td>
</tr>
<tr>
<td>Drain-Source On-State Resistance</td>
<td>R_DDS(on)</td>
<td>V_GS = 10 V, I_D = 0.3 A</td>
<td>2.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_GS = 4.5 V, I_D = 0.2 A</td>
<td>2.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_GS = 2.5 V, I_D = 0.1 A</td>
<td>2.4</td>
</tr>
<tr>
<td>Forward Transconductance</td>
<td>g_fs</td>
<td>V_DS = 10 V, I_D = 0.3 A</td>
<td>1.6</td>
</tr>
<tr>
<td>Diode Forward Voltage</td>
<td>V_SD</td>
<td>V_GS = 0 V, I_S = 0.3 A</td>
<td>0.8</td>
</tr>
<tr>
<td><strong>Dynamic</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Gate Charge</td>
<td>Q_g</td>
<td>V_DS = 192 V, V_GS = 10 V, I_D = 0.5 A</td>
<td>4.87</td>
</tr>
<tr>
<td>Gate-Source Charge</td>
<td>Q_gps</td>
<td></td>
<td>0.56</td>
</tr>
<tr>
<td>Gate-Drain Charge</td>
<td>Q_ggd</td>
<td></td>
<td>1.53</td>
</tr>
<tr>
<td>Turn-On Delay Time</td>
<td>t_(on)</td>
<td>V_DD = 60 V, R_L = 200 Ω</td>
<td>5</td>
</tr>
<tr>
<td>Rise Time</td>
<td>t_r</td>
<td>I_D = 0.3 A, V_GEN = 10 V, R_g = 25 Ω</td>
<td>12</td>
</tr>
<tr>
<td>Turn-Off Delay Time</td>
<td>t_(off)</td>
<td></td>
<td>35</td>
</tr>
<tr>
<td>Fail Time</td>
<td>t_f</td>
<td></td>
<td>16</td>
</tr>
</tbody>
</table>

Notes:

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

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**Output Characteristics**

- **On-Resistance vs. Drain Current**
  - $V_{GS} = 10 \text{ thru } 3 \text{ V}$
  - $2.5 \text{ V}$
  - $2 \text{ V}$
  - $V_{DS}$ vs. $I_D$ (A)

- **Gate Charge**
  - $V_{GS} = 4.5 \text{ V}$
  - $V_{GS} = 10 \text{ V}$
  - $R_{DS(on)}$ vs. $I_D$ (A)

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**Transfer Characteristics**

- **Capacitance**
  - $V_{GS} = 4.5 \text{ V}$
  - $ID = 0.2 \text{ A}$
  - $V_{DS}$ vs. $V_{GS}$ (V)

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**On-Resistance vs. Drain Current**

- $V_{DS} = 192 \text{ V}$
- $I_D = 0.5 \text{ A}$

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**Gate Charge**

- $Q_G$ vs. $V_{GS}$ (Gate-to-Source Voltage) (V)

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**On-Resistance vs. Junction Temperature**

- $R_{DS(on)}$ vs. $T_J$ (Junction Temperature) (°C)

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*Vishay Siliconix*

For technical questions, contact: pmostechsupport@vishay.com

www.vishay.com
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient
(TO-236, TN2404K only)

- Duty Cycle, D = \frac{t_1}{t_2}
- Per Unit Base = R_{thJA} = 350°C/W
- TJ, - TA = P_{Dm}Z_{thJA}(t)
- Surface Mounted

Normalized Thermal Transient Impedance, Junction-to-Ambient
(TO-226AA, TN2404KL and TO-92-18RM, BS107KL only)

- Duty Cycle, D = \frac{t_1}{t_2}
- Per Unit Base = R_{thJA} = 156°C/W
- TJ, - TA = P_{Dm}Z_{thJA}(t)
- Surface Mounted
## Package Information

**Vishay Siliconix**

### SOT-23 (TO-236): 3-LEAD

![Diagram of SOT-23 (TO-236) Package]

### Dimensions Table

<table>
<thead>
<tr>
<th>Dim</th>
<th>MILLIMETERS</th>
<th>INCHES</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.89 - 1.12</td>
<td>0.035 - 0.044</td>
</tr>
<tr>
<td>A₁</td>
<td>0.01 - 0.10</td>
<td>0.0004 - 0.004</td>
</tr>
<tr>
<td>A₂</td>
<td>0.88 - 1.02</td>
<td>0.0346 - 0.040</td>
</tr>
<tr>
<td>b</td>
<td>0.35 - 0.50</td>
<td>0.014 - 0.020</td>
</tr>
<tr>
<td>c</td>
<td>0.085 - 0.18</td>
<td>0.003 - 0.007</td>
</tr>
<tr>
<td>D</td>
<td>2.80 - 3.04</td>
<td>0.110 - 0.120</td>
</tr>
<tr>
<td>E</td>
<td>2.10 - 2.64</td>
<td>0.083 - 0.104</td>
</tr>
<tr>
<td>E₁</td>
<td>1.20 - 1.40</td>
<td>0.047 - 0.055</td>
</tr>
<tr>
<td>e</td>
<td>0.95 BSC</td>
<td>0.0374 Ref</td>
</tr>
<tr>
<td>e₁</td>
<td>1.90 BSC</td>
<td>0.0748 Ref</td>
</tr>
<tr>
<td>L</td>
<td>0.40 - 0.60</td>
<td>0.016 - 0.024</td>
</tr>
<tr>
<td>L₁</td>
<td>0.64 Ref</td>
<td>0.025 Ref</td>
</tr>
<tr>
<td>S</td>
<td>0.50 Ref</td>
<td>0.020 Ref</td>
</tr>
<tr>
<td>q</td>
<td>3° - 8°</td>
<td>3° - 8°</td>
</tr>
</tbody>
</table>

**ECN:** S-03946-Rev. K, 09-Jul-01

**DWG:** 5479
Mounting LITTLE FOOT® SOT-23 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs, (http://www.vishay.com/doc?72286), for the basis of the pad design for a LITTLE FOOT SOT-23 power MOSFET footprint. In converting this footprint to the pad set for a power device, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

The electrical connections for the SOT-23 are very simple. Pin 1 is the gate, pin 2 is the source, and pin 3 is the drain. As in the other LITTLE FOOT packages, the drain pin serves the additional function of providing the thermal connection from the package to the PC board. The total cross section of a copper trace connected to the drain may be adequate to carry the current required for the application, but it may be inadequate thermally. Also, heat spreads in a circular fashion from the heat source. In this case the drain pin is the heat source when looking at heat spread on the PC board.

Figure 1 shows the footprint with copper spreading for the SOT-23 package. This pattern shows the starting point for utilizing the board area available for the heat spreading copper. To create this pattern, a plane of copper overlies the drain pin and provides planar copper to draw heat from the drain lead and start the process of spreading the heat so it can be dissipated into the ambient air. This pattern uses all the available area underneath the body for this purpose.

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, “thermal” connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low-impedance path for heat to move away from the device.
RECOMMENDED MINIMUM PADS FOR SOT-23
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